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MS-7B28

ATX:234mm*185mm

Intel -CoffeeLake-S plamform

CPU:

LGA1151

CPU POWER PAK *4Phase

GT POWER PAK *2 Phase

Onboard Chip:

SIO: NUVOTON 5567

HD Audio Codec: ALC887

LAN: INTEL I219V

Flash ROM: SPI 64 MB

CUT VBAT:SLG4B41231

Main Memory:

DDR4 * 2 (Dual Channel)

ACPI:

5VDAUL:uP7501

5VDIMM:uP7501

3VSB:GS7133+N MOS

1P8_VSB:GS7166

3VDSW:L11831

VCCSTPLL:GS7133

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

System Chipset:

H310

PWM:

VCORE - RT3607	138A
VGT- RT3607	45A
DDR - RT8231	11.525A
DDR VPP25- MP2143	1.12A
PCH(1.05V) - RT8125E	10.743A
VCCSA - RT8125E	11.1A
VCCIO - SY8288	6.4A

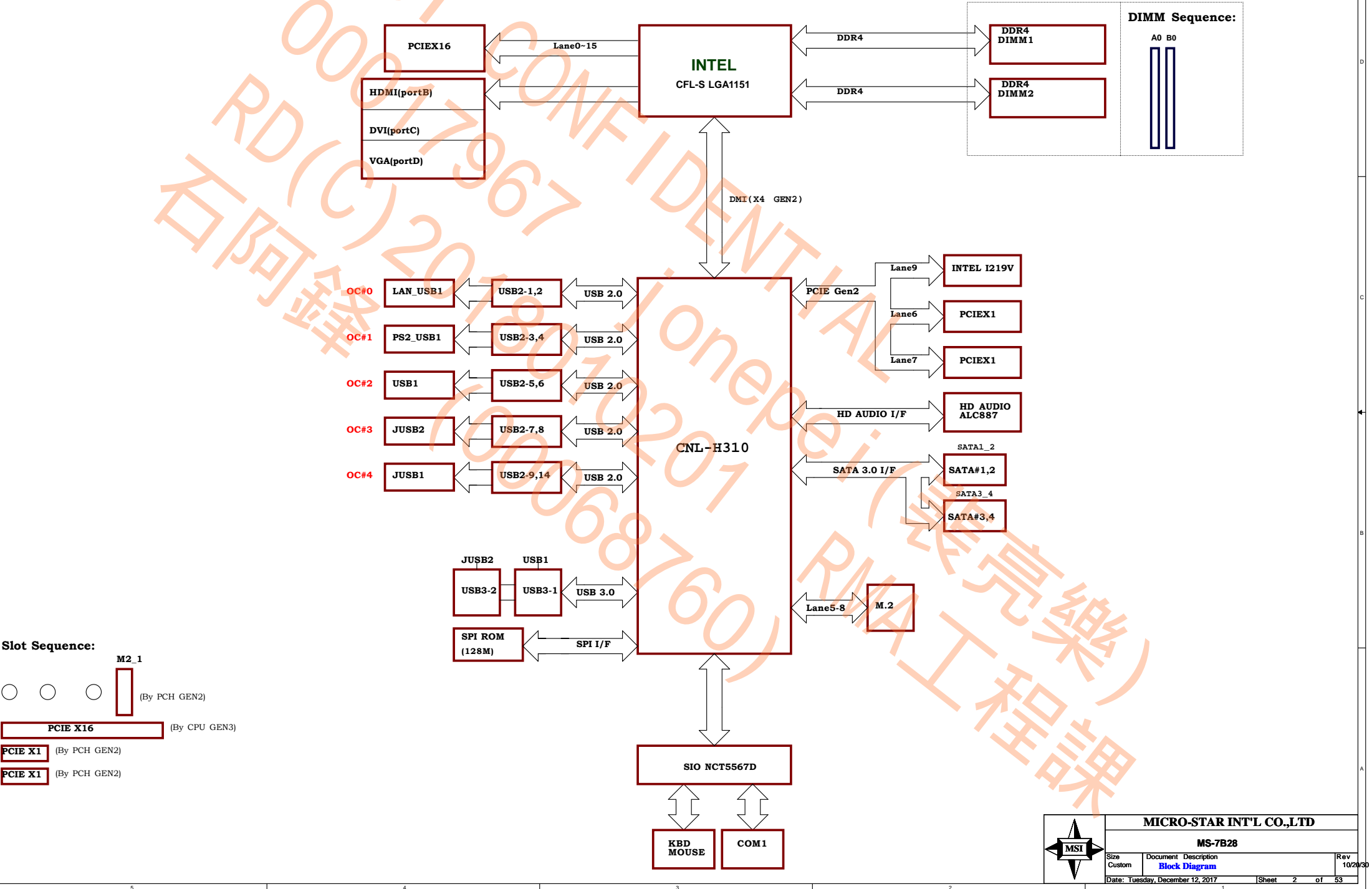


MICRO-STAR INT'L CO.,LTD

MS-7B28

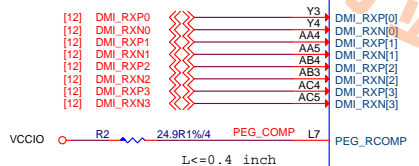
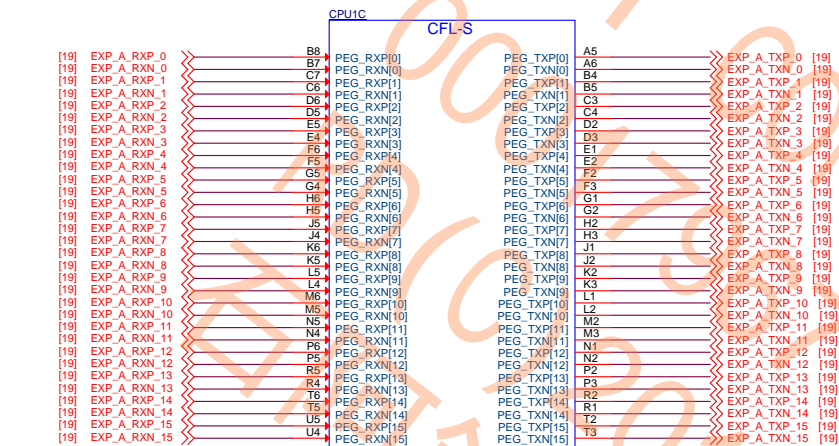
Size	Document	Description	Rev
Custom	Cover Sheet		10/20/30
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Block Diagram

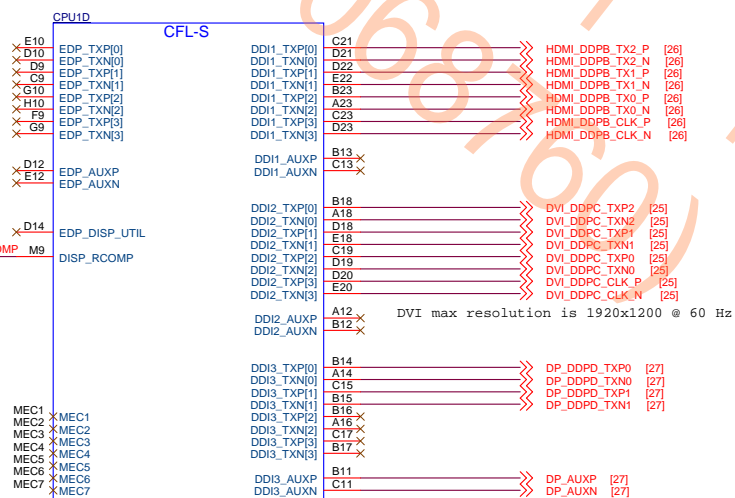




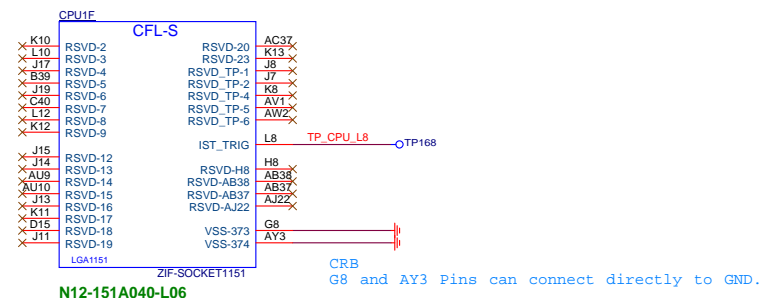
Size Custom	Document Description CPU-Memory	Rev 10/20/30
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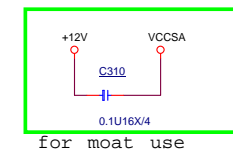
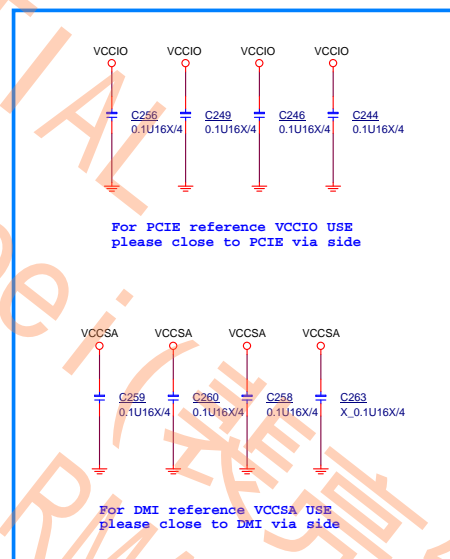
N12-151A040-L06



N12-151A040-L06



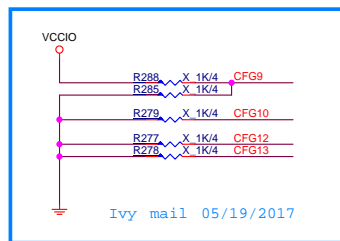
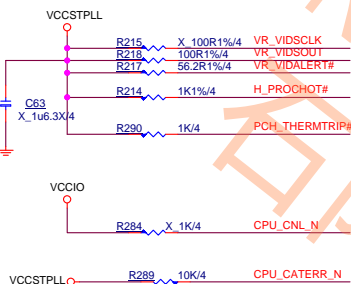
N12-151A040-L06



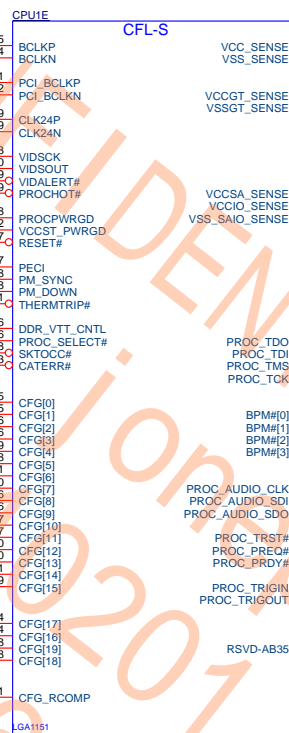
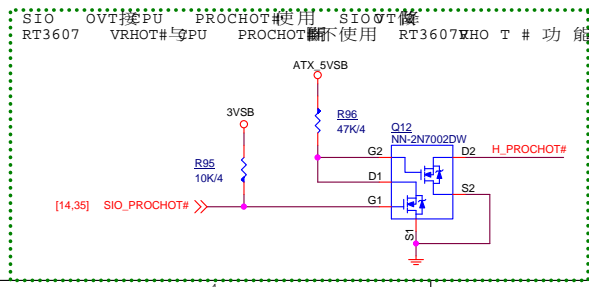
MICRO-STAR INT'L CO.,LTD

MS-7B28

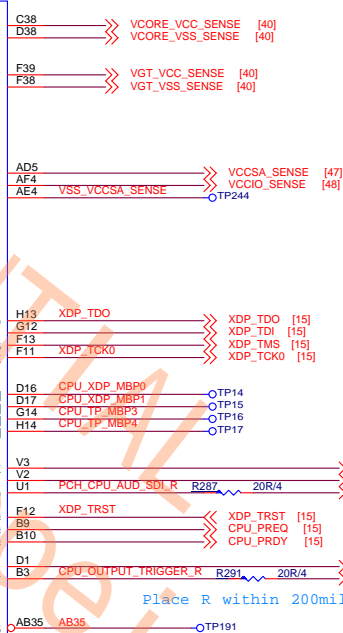
Size	Document	Description	Rev
Custom		CPU-PEG/Display	10/20/30
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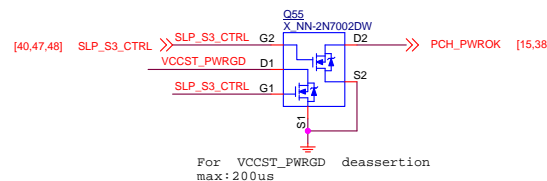
CFG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL Lock
1			RSVD
2	NORM	REVERSE	REQ_LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PGOCFGSEL[0]
6	DISABLE	ENABLE	PGOCFGSEL[1]
7	RESET#	BIOS REQ	REQ_DEFER_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		RSVD
15	RSVD		RSVD



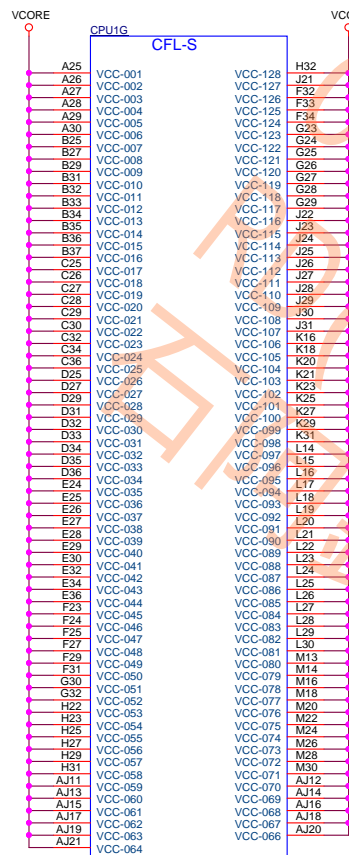
N12-151A040-L06



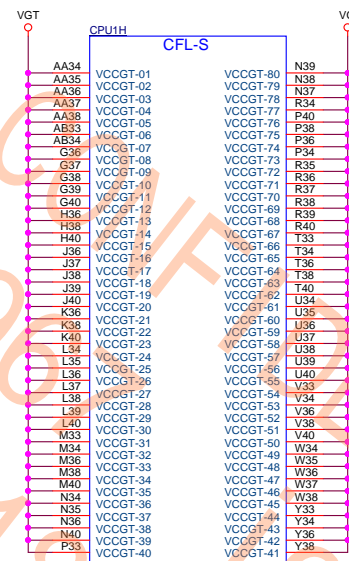
POWER DOWN-板拿掉



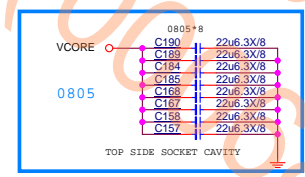
MICRO-STAR INT'L CO.,LTD			
MS-7B28			
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Custom		CPU-Control/MISC/CFG/Audio	10/20/30
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LGA1151
ZIF-SOCKET1151
N12-151A040-L06

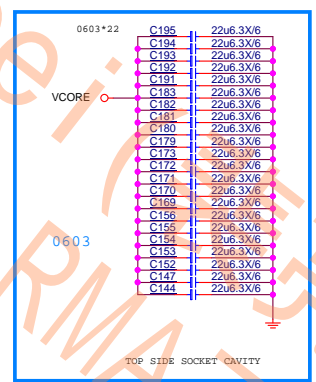


LGA1151
ZIF-SOCKET1151
N12-151A040-L06



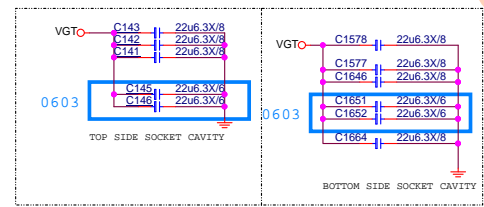
0805

TOP SIDE SOCKET CAVITY



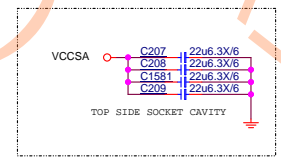
0603

TOP SIDE SOCKET CAVITY

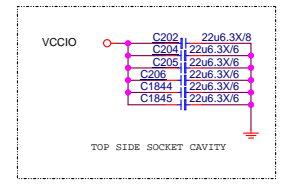


0603

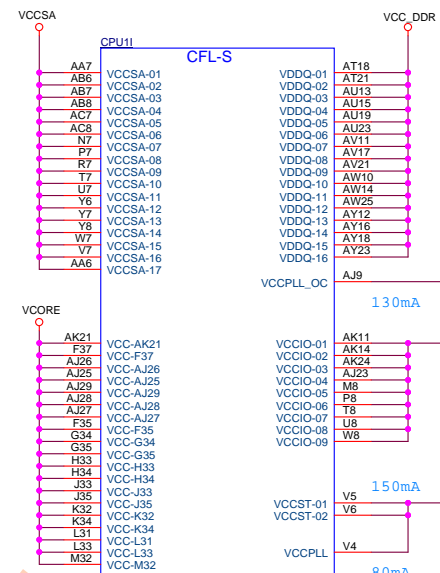
BOTTOM SIDE SOCKET CAVITY



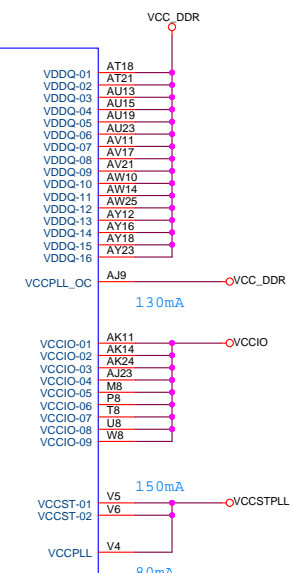
TOP SIDE SOCKET CAVITY



TOP SIDE SOCKET CAVITY



LGA1151
ZIF-SOCKET1151
N12-151A040-L06



130mA

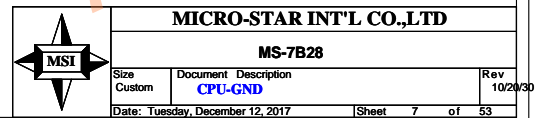
150mA

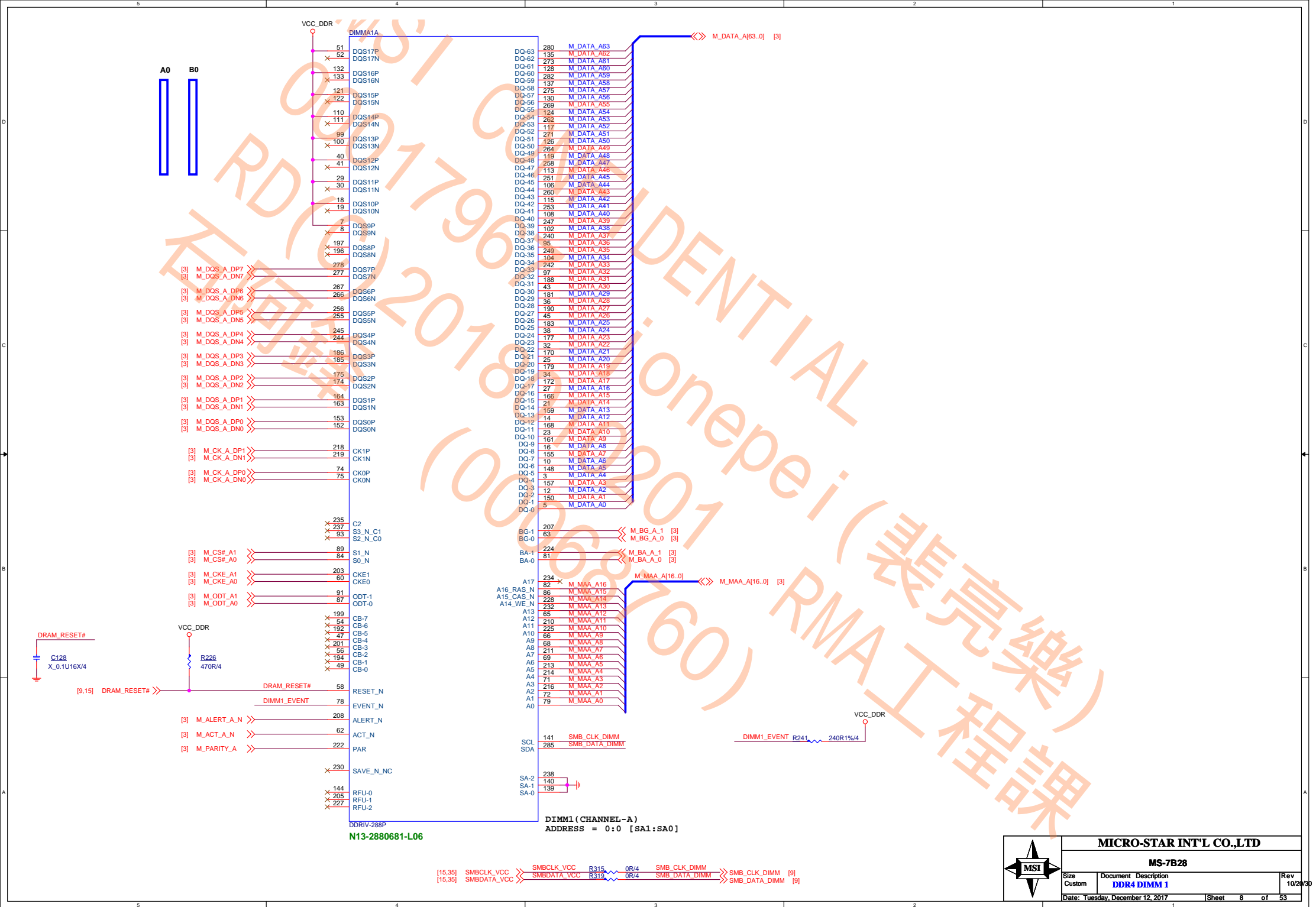
80mA

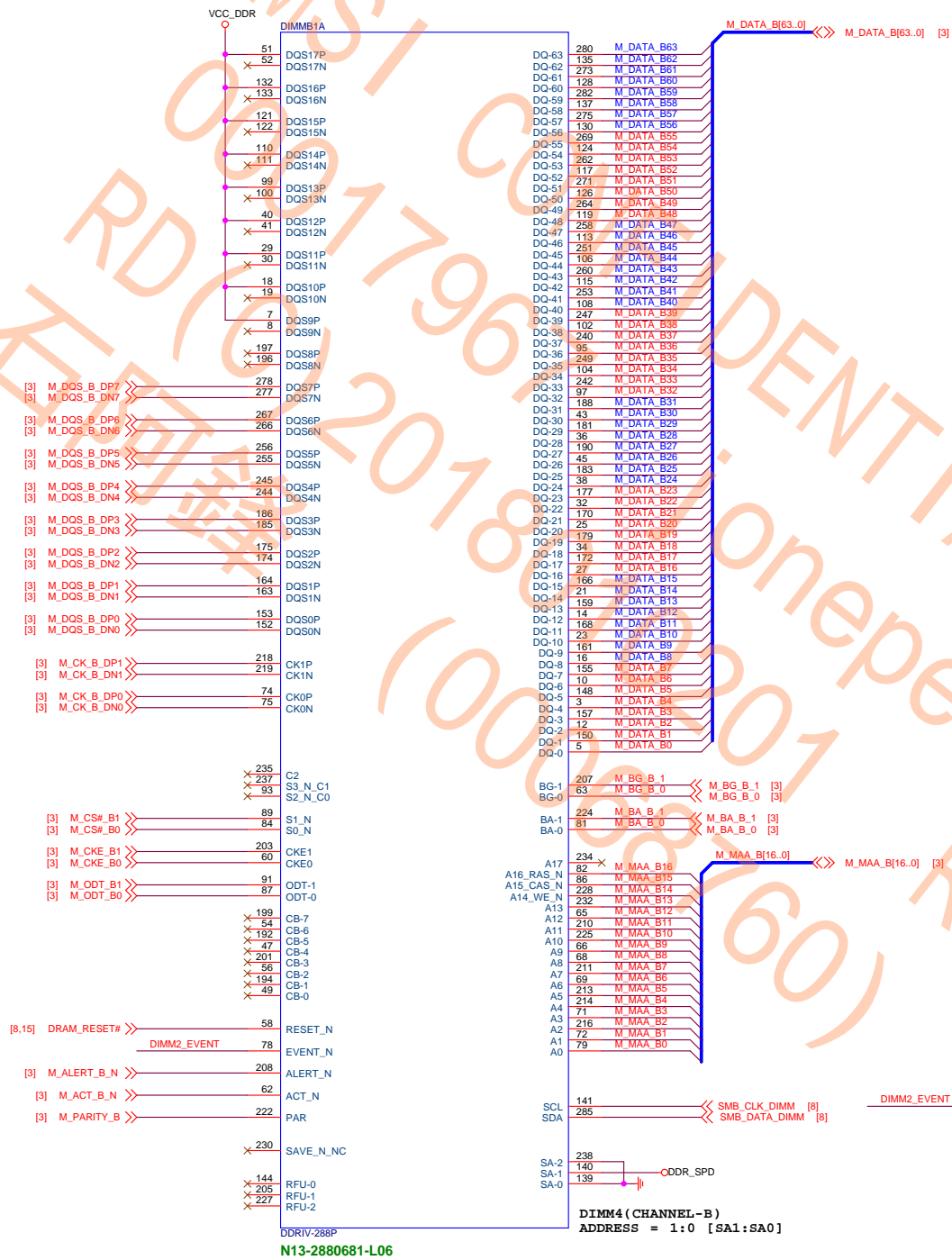
CBB/MLCC in CPU Socket Left VCC_DDR, TOP SIDE between SOCKET and DIMM Slot.

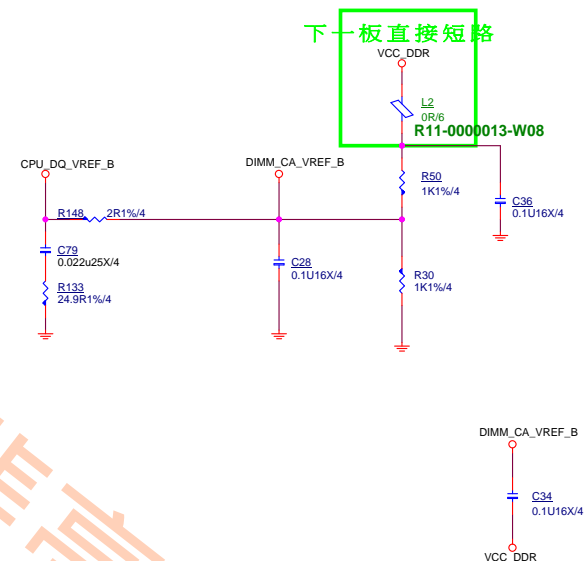
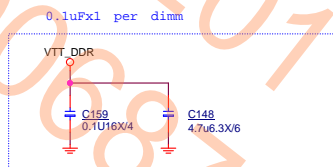
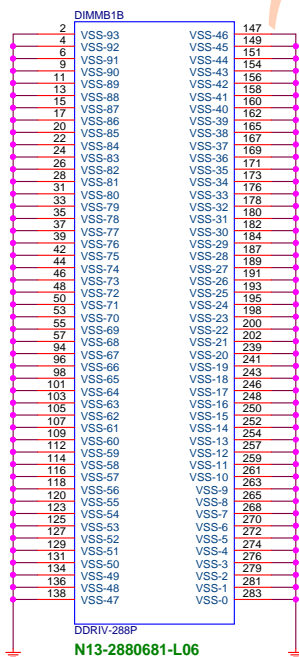
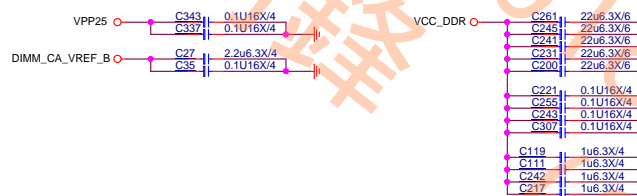
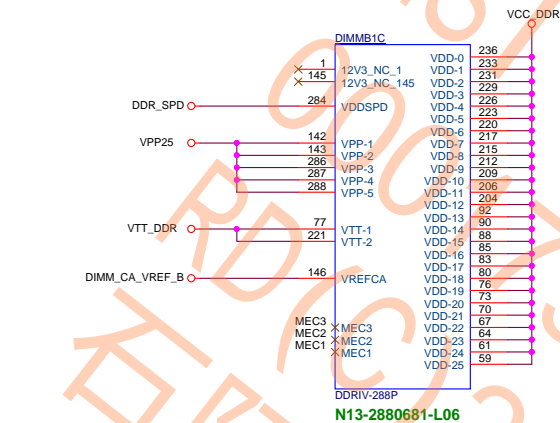
CBB/MLCC in CPU Socket Left VCC_DDR, TOP SIDE between SOCKET and DIMM Slot.

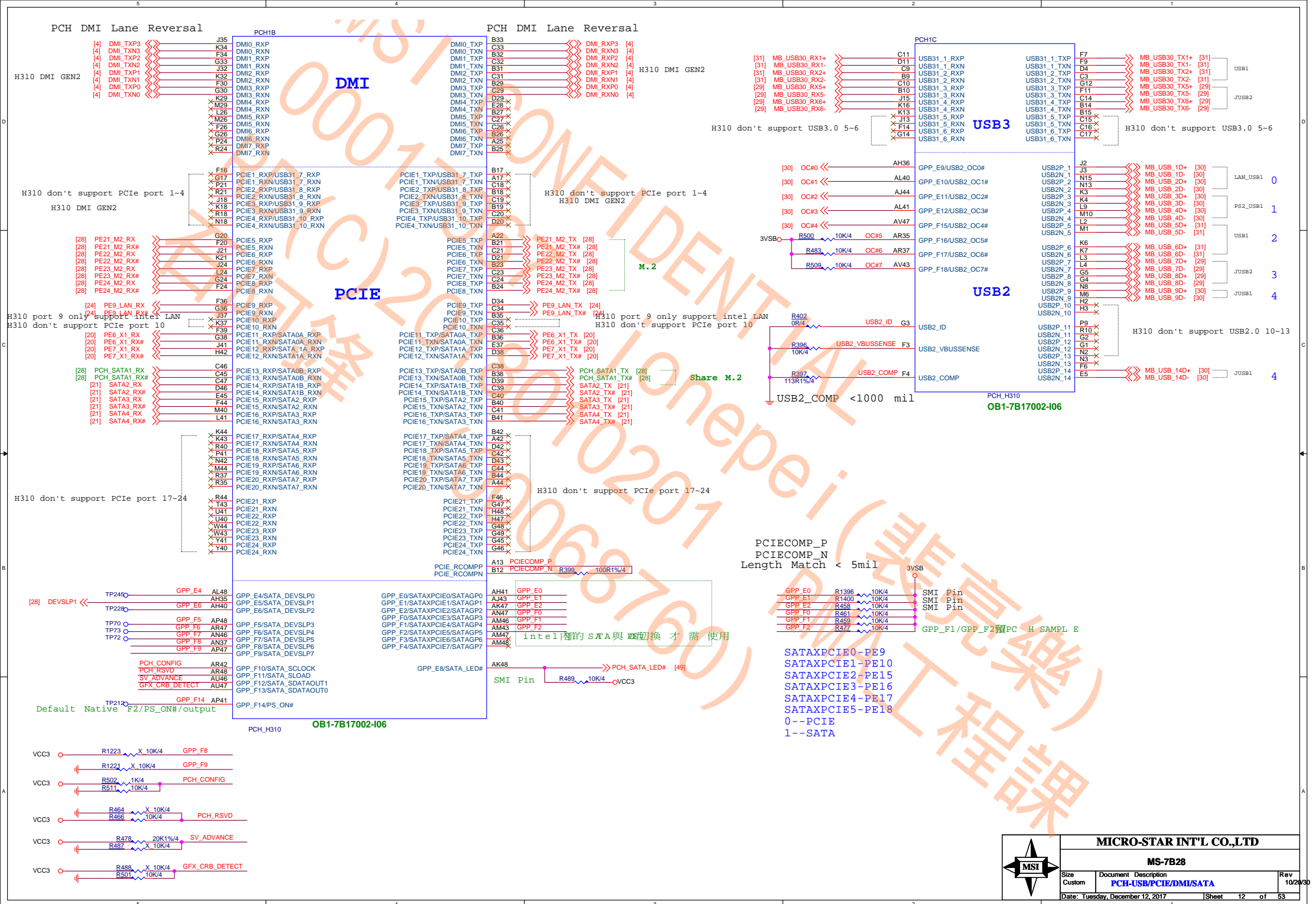
CBB/MLCC in CPU Socket Left VCC_DDR, TOP SIDE between SOCKET and DIMM Slot.



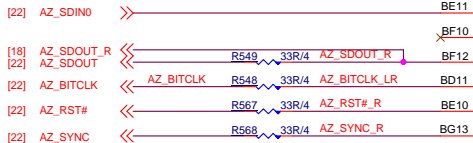
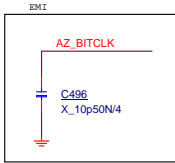
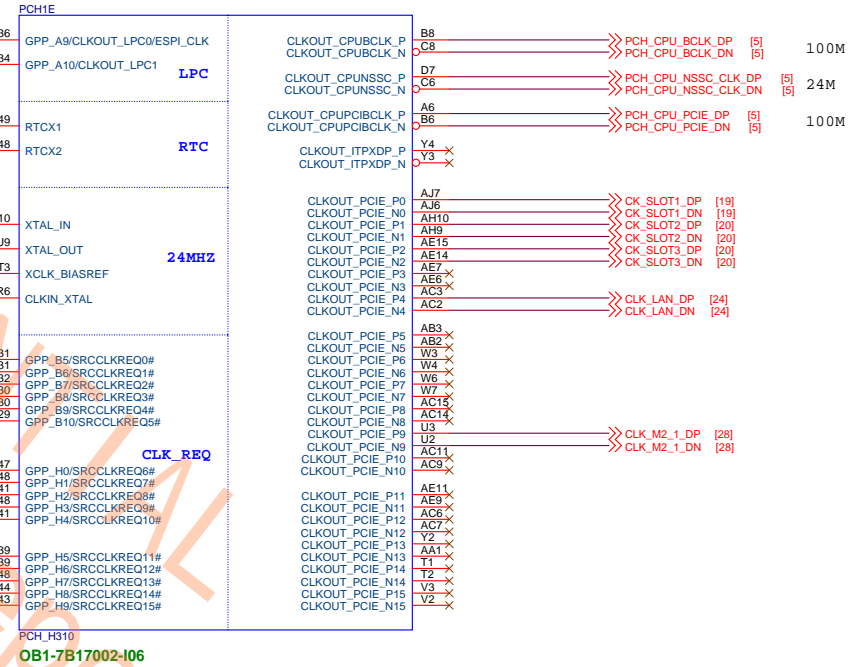
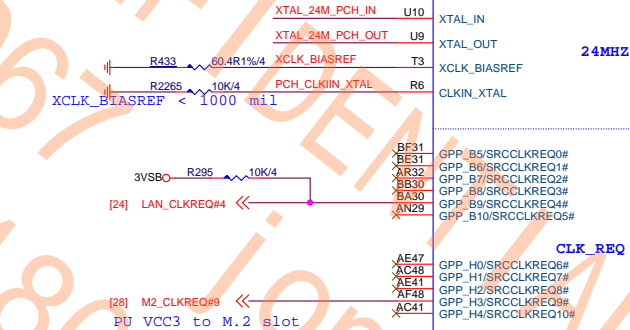
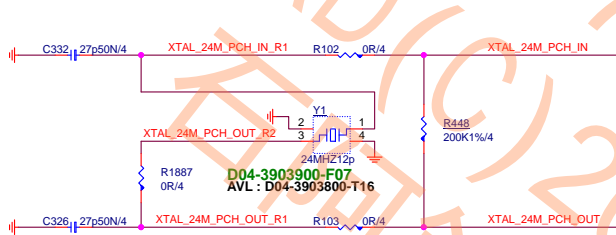
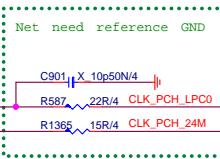
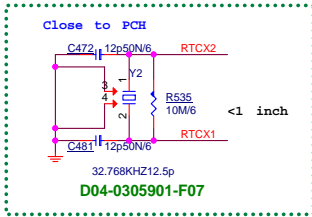






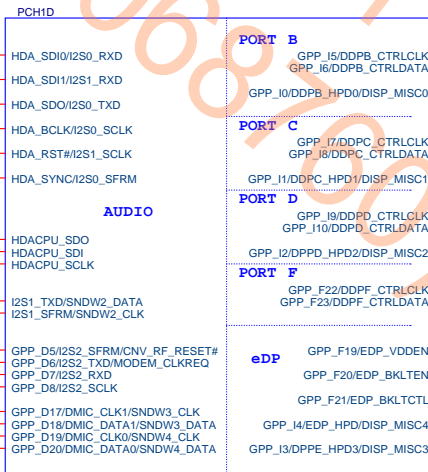


RTC Block

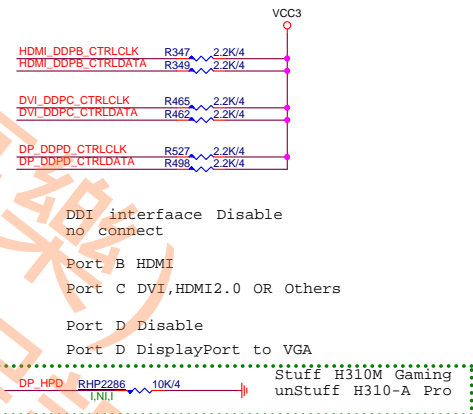
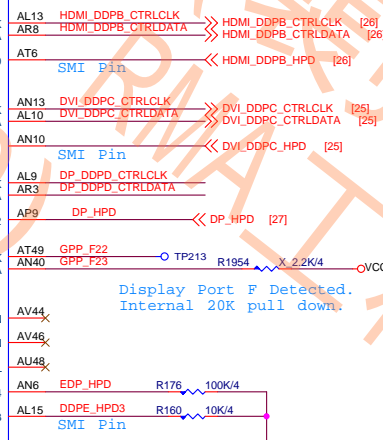


Default Native F3/CNV_RF_R_ESET#.

Default Native F3/MODEM_CLKREQ.

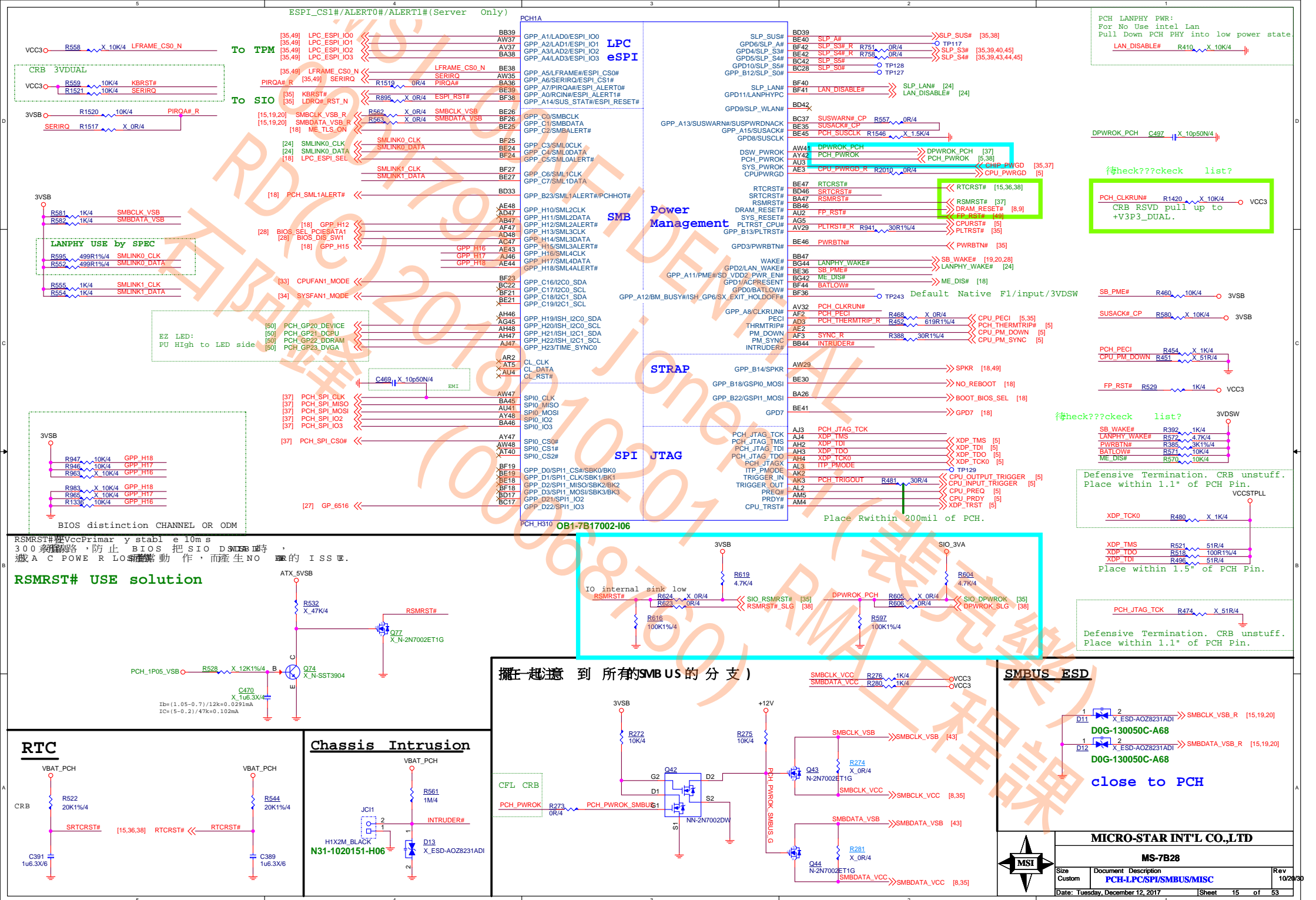


PCH_H310
OB1-7B17002-106



Schematic Cfg	Project
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	V A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	X B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	V C

MICRO-STAR INT'L CO.,LTD			
MS-7B28			
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Custom		PCH-Audio/Display/Clock	10/20/30
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VSS

OB1-7B17002-I06

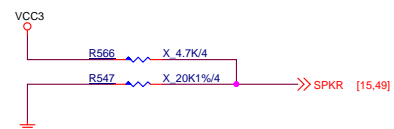


MICRO-STAR INT'L CO.,LTD

MS-7B28

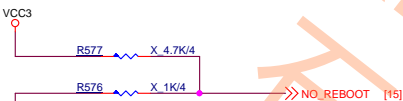
Size	Document	Description	Rev
Custom		PCH-GND	10/20/00
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TOP Swap



Internal pull-down 20K is disabled after PLTRST#

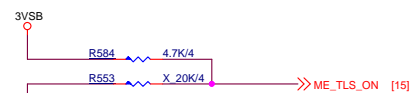
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

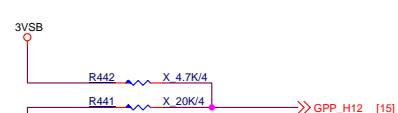
AMT and SBA with confidentiality



0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

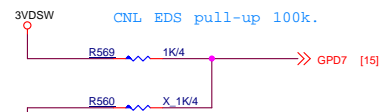
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

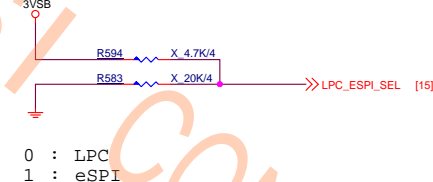
Internal pull-down 20K is disabled after RSMRST

Reserved



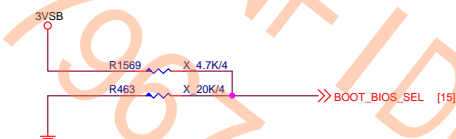
XTAL INPUT MODE
0 = XTAL INPUT IS SINGLE-ENDED
1 = XTAL INPUT IS DIFFERENTIAL
PCH HAS INTERNAL 20K PD

LPC eSPI Mode



0 : LPC
1 : eSPI

Boot BIOS

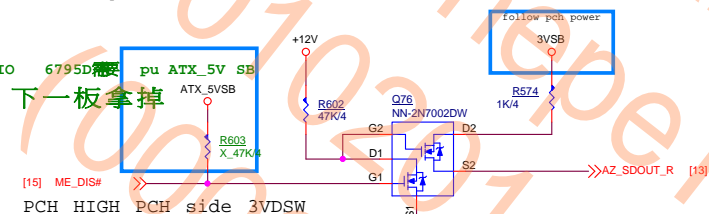


0 : SPI
1 : LPC

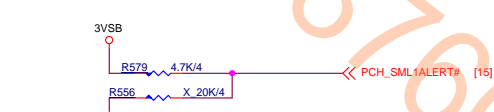
Internal pull-down 20K is disabled after PLTRST

HDA_SDO

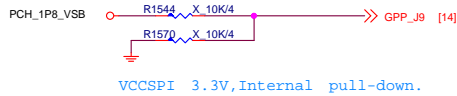
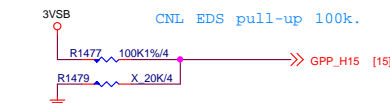
ME flash by GPIO



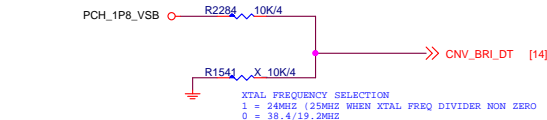
Reserved



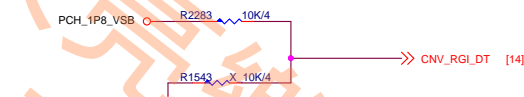
Reserved



VCCSPI 3.3V, Internal pull-down.
SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE
0 = VCCSPI IS CONNECTED TO 3.3V RAIL - DEFAULT
1 = VCCSPI IS CONNECTED TO 1.8V RAIL
PCH HAS INTERNAL 20K PD



XTAL FREQUENCY SELECTION
1 = 24MHZ (25MHZ WHEN XTAL FREQ DIVIDER NON ZERO)
0 = 38.4/19.2MHZ



CNL EDS
1 = Integrated CNVi enable
0 = Integrated CNVi disable



MICRO-STAR INT'L CO.,LTD

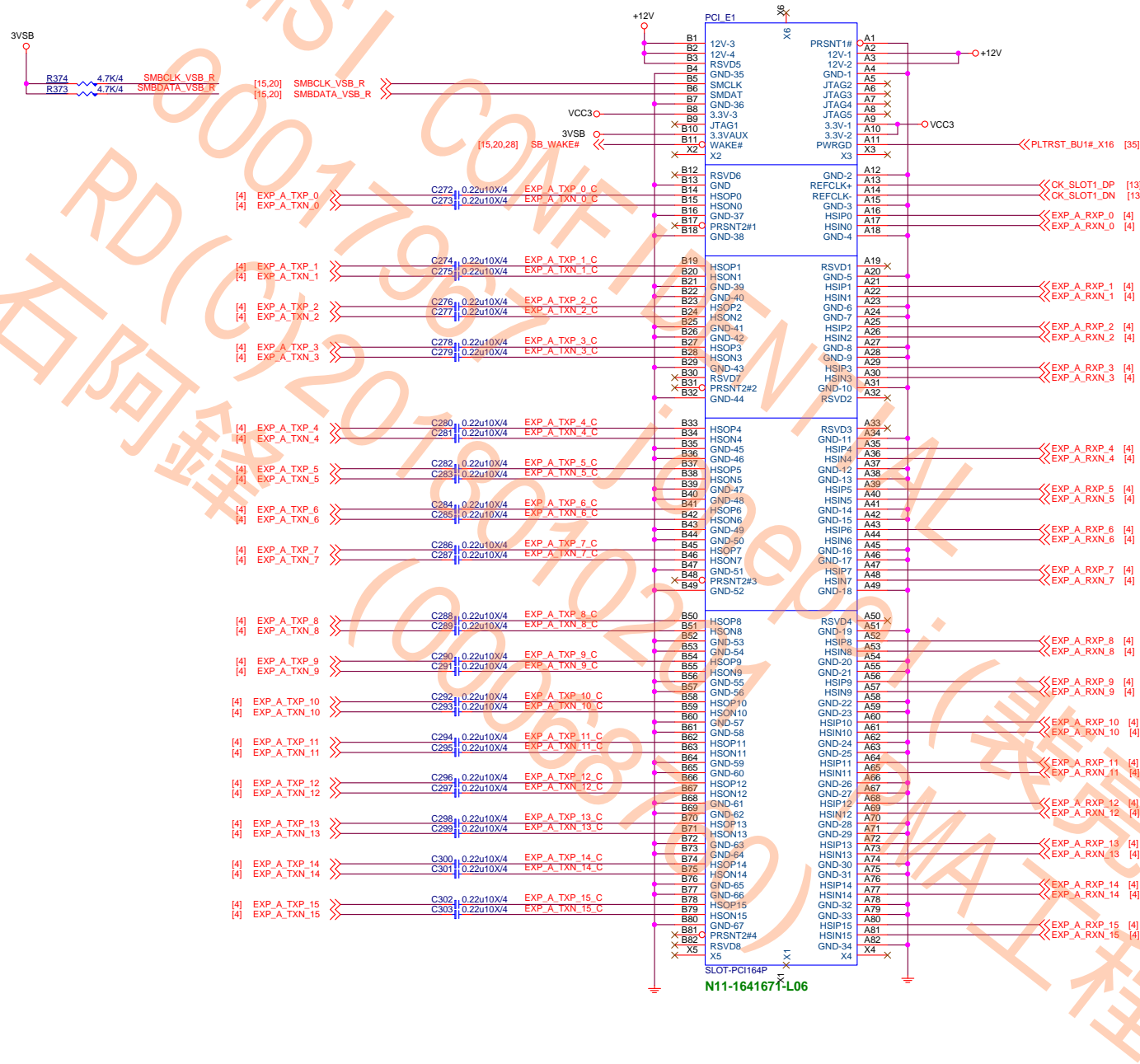
MS-7B28

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Custom		PCH-Strap	10/2/30
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C71-2711761-N07

C71-5610671-N07

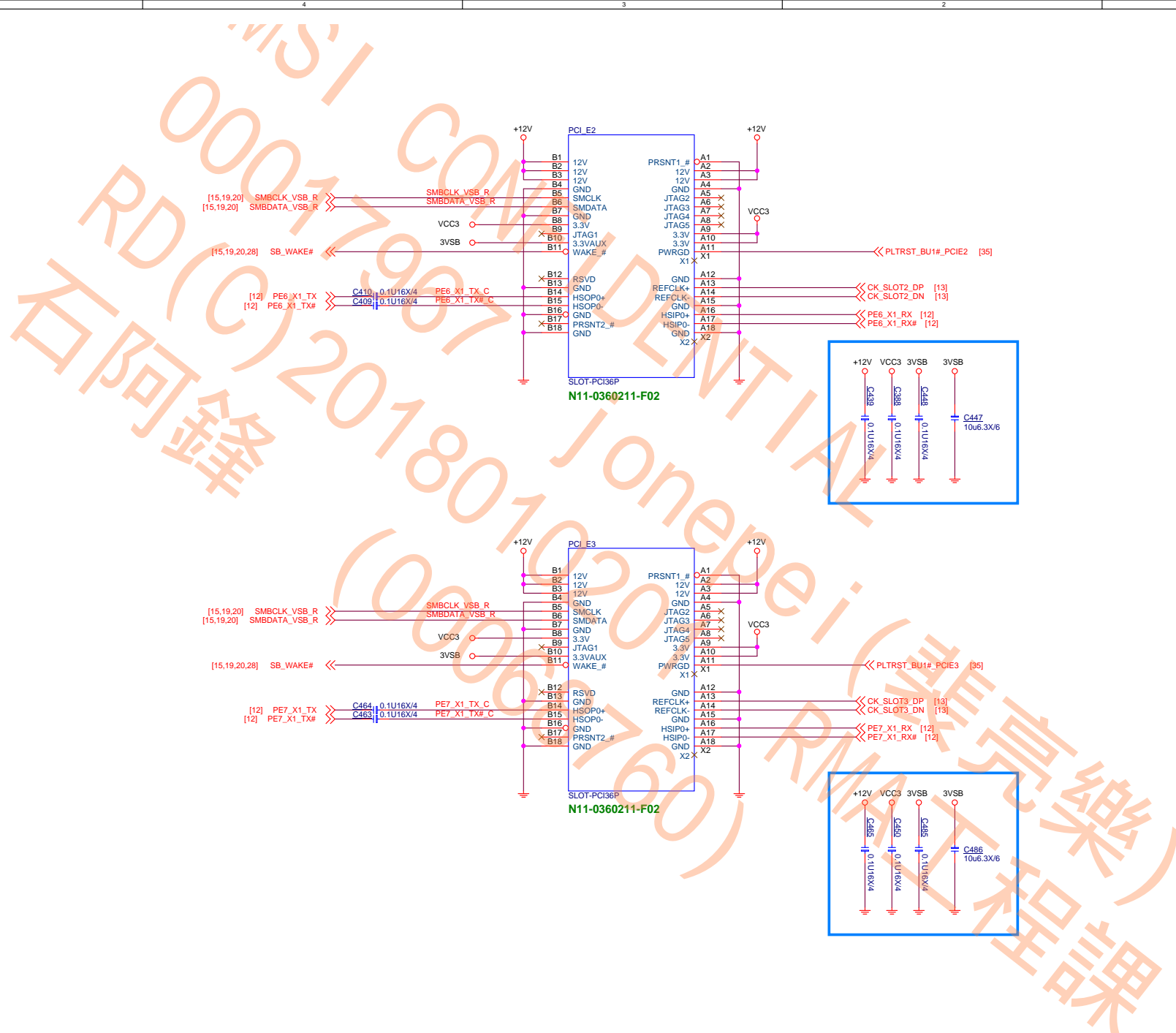
C394 10u6.3X/6



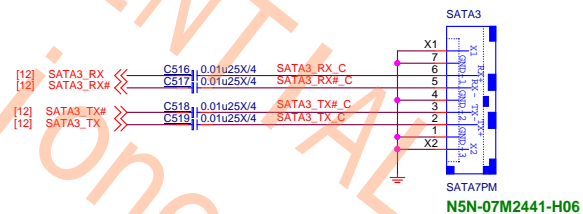
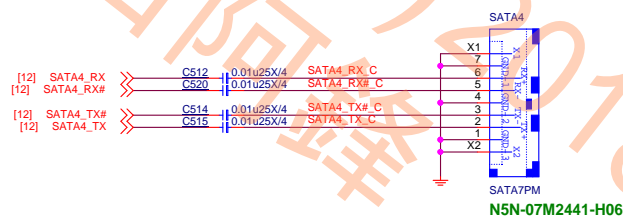
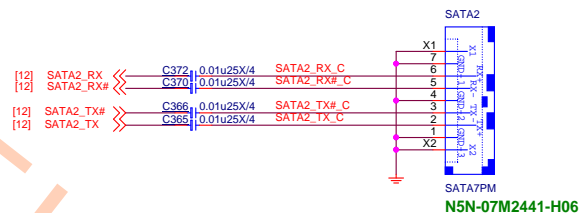
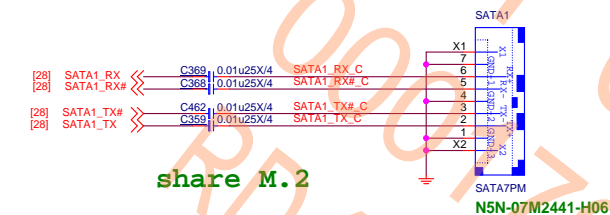
MICRO-STAR INT'L CO.,LTD

MS-7B28

Size	Document	Description	Rev
Custom		PCIE SLOT-CPU(X16)	10/20/30
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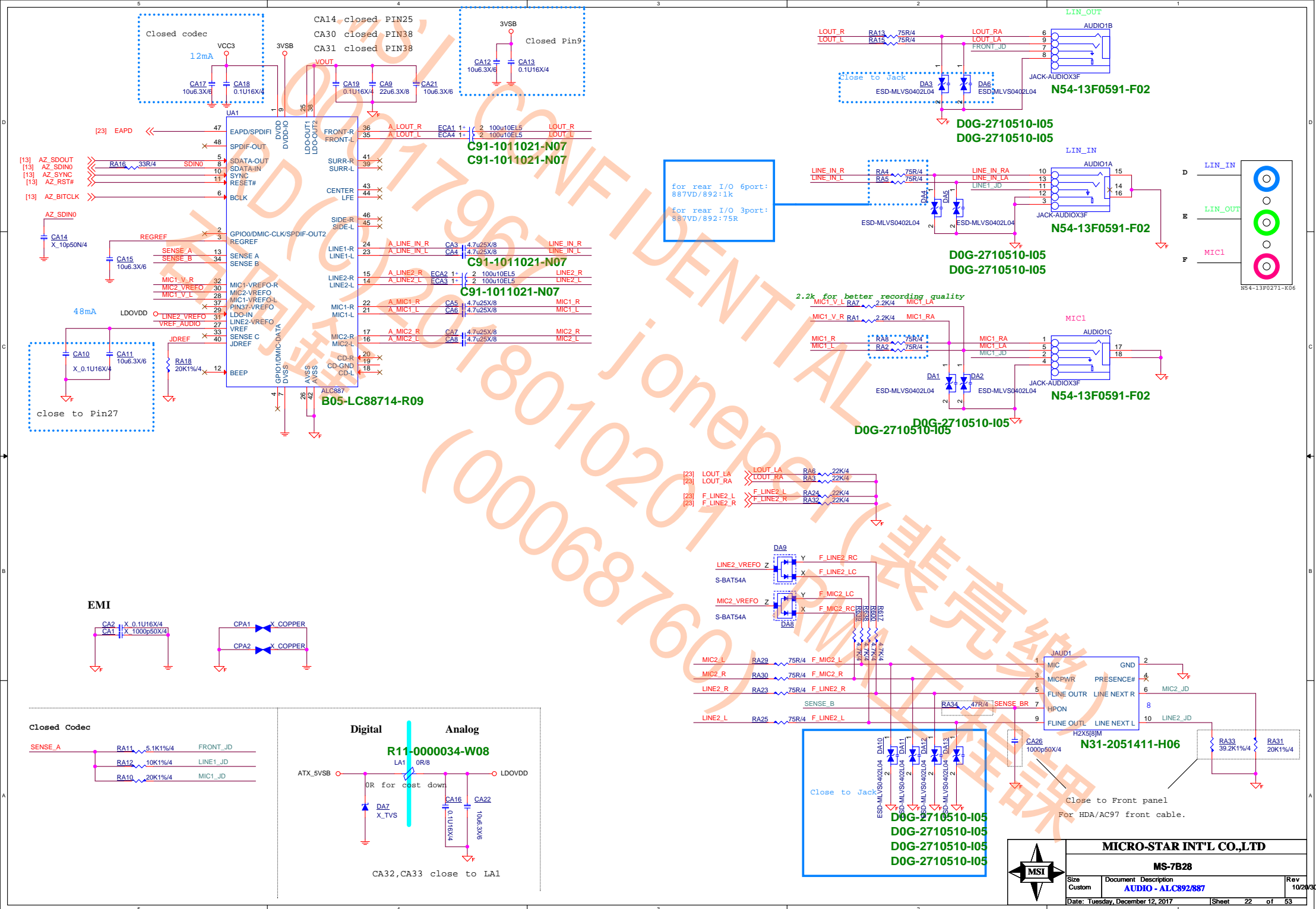
SATA 6G



MICRO-STAR INT'L CO.,LTD

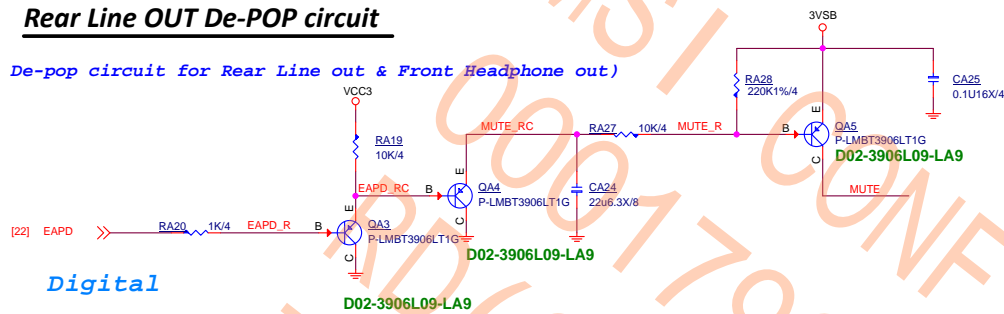
MS-7B28

Size	Document	Description	Rev
Custom		SATA connector	10/2/30
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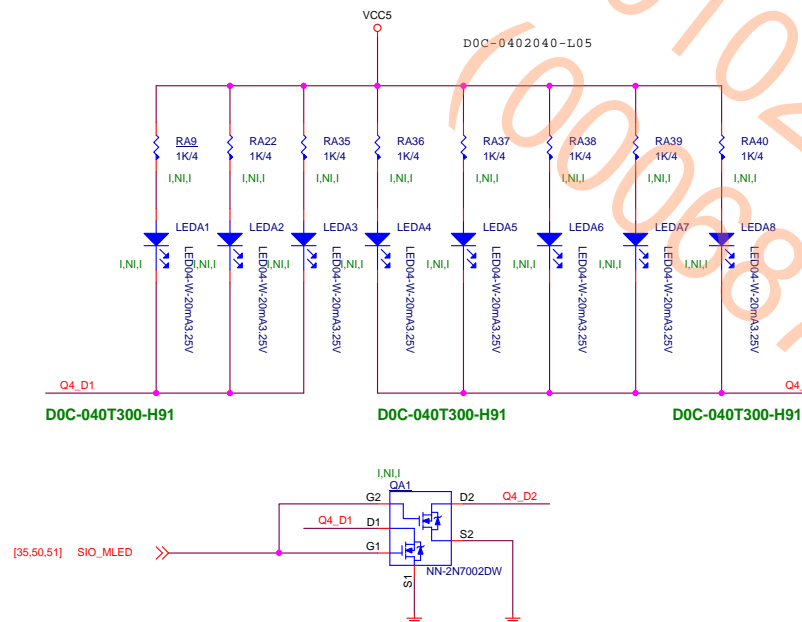


Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Audio LED



Schematic Cfg	Project	
CFG1-7B38-H310 (H310M GAMING PLUS)	ver.1.0	V A
CFG1-7B38-H310-APRO (H310-A Pro)	ver.2.0	X B
CFG1-7B38-H310 (H310-A GAMING ARCTIC)	ver.3.0	V C

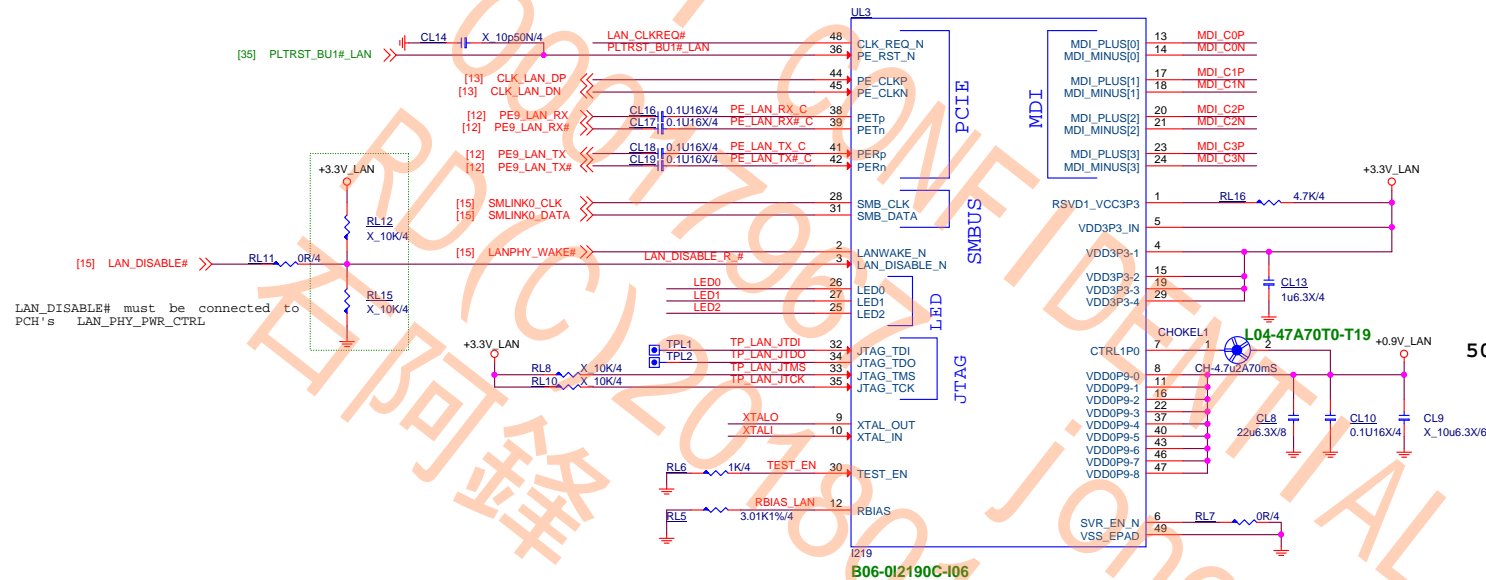


MICRO-STAR INT'L CO.,LTD

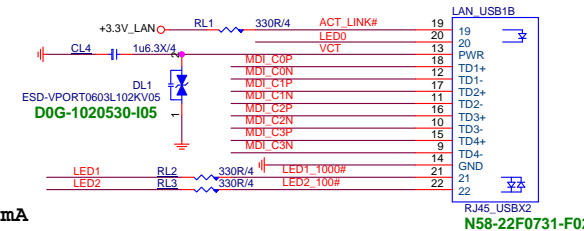
MS-7B28

Size	Document	Description	Rev
Custom		AUDIO - depop circuit	10/20/30
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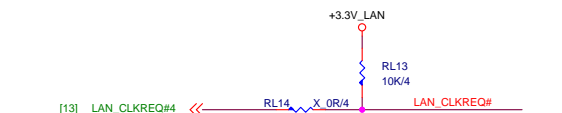
Intel Lan- I219



LAN Connector

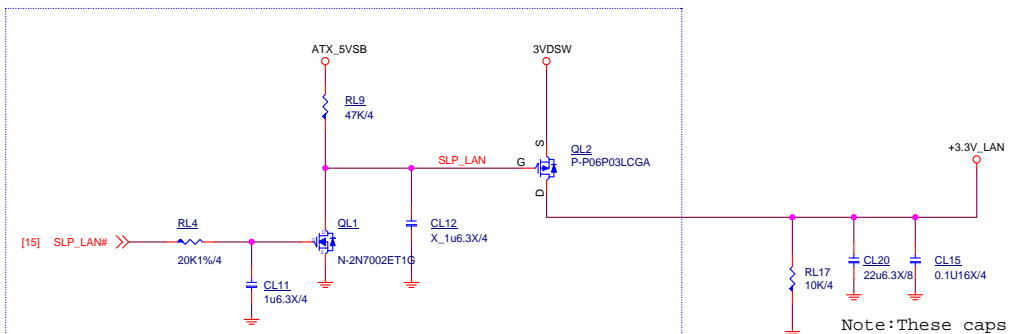


PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN



The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

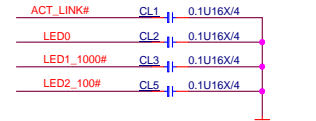
support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



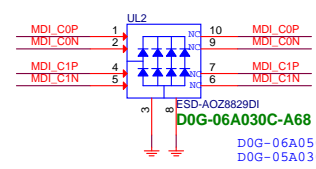
+3.3V LAN
I219: 542mW

Note: These caps closed to PHY

For EMI



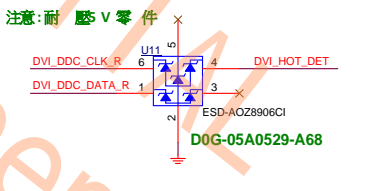
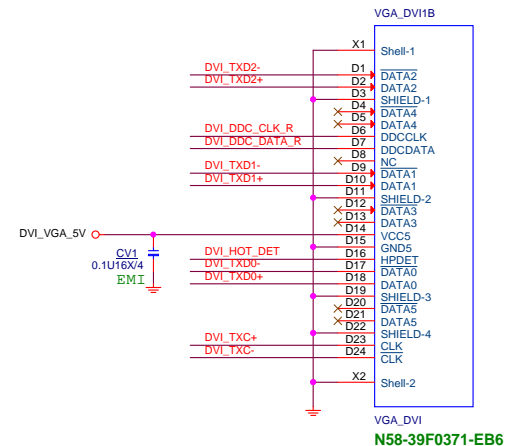
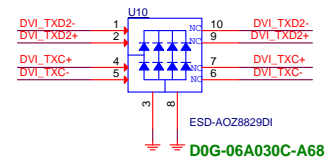
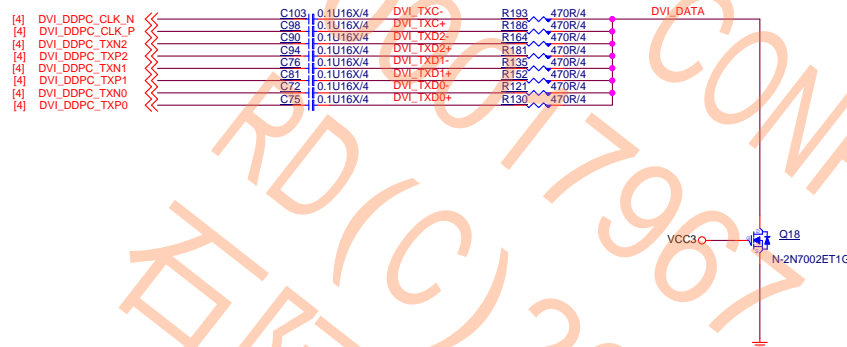
UL2&UL3 close to connector



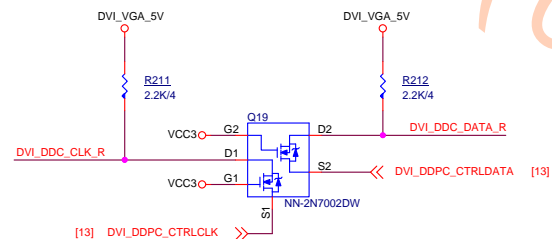
Do not pair MDI0 and MDI1 on the same TVSdevice
(avoid LAN POE connecting issue).
Otherpairing combination is ok.

DVI level shifter

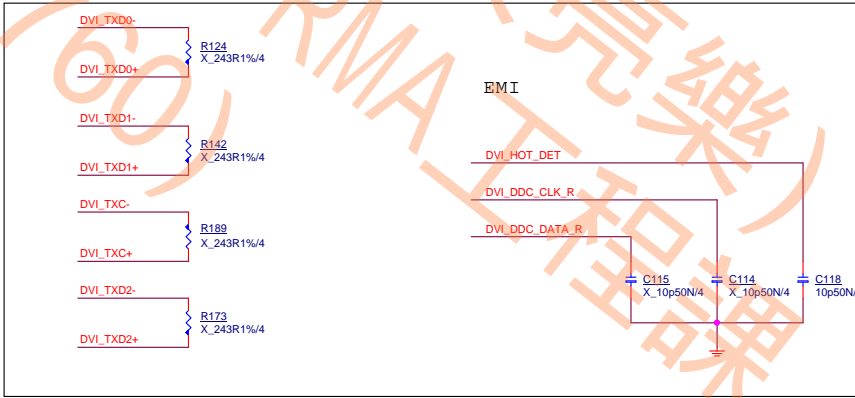
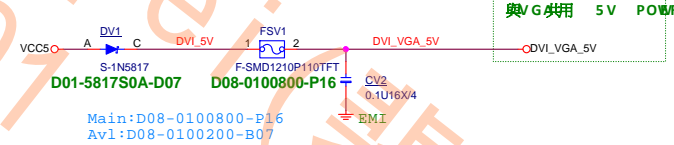
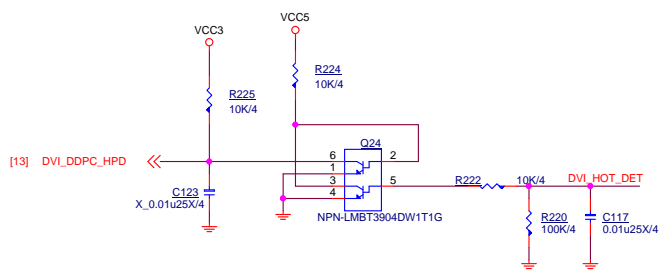
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



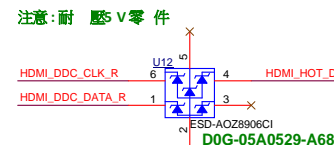
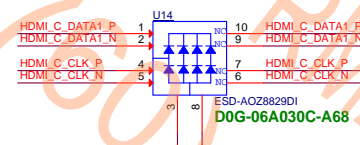
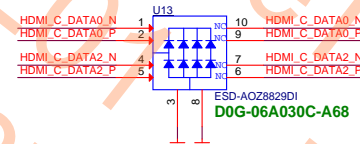
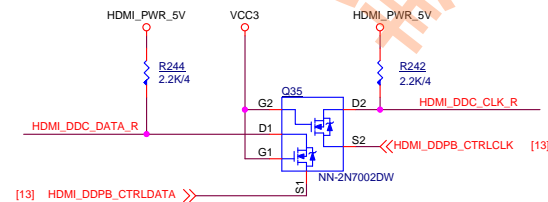
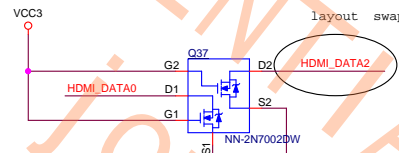
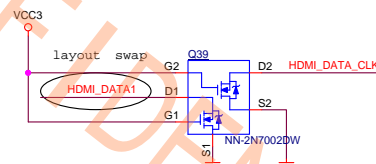
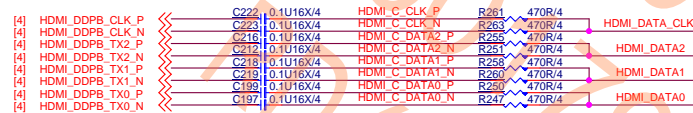
LEVEL SHIFTER using I2C Repeater



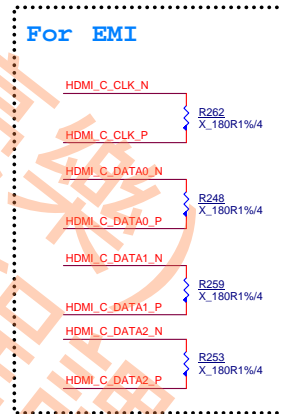
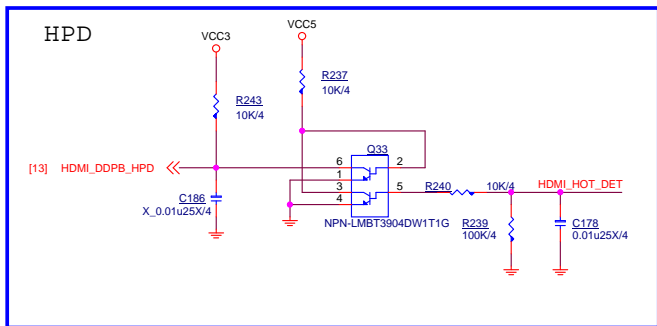
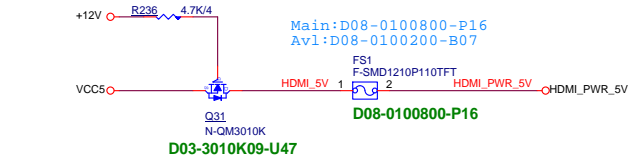
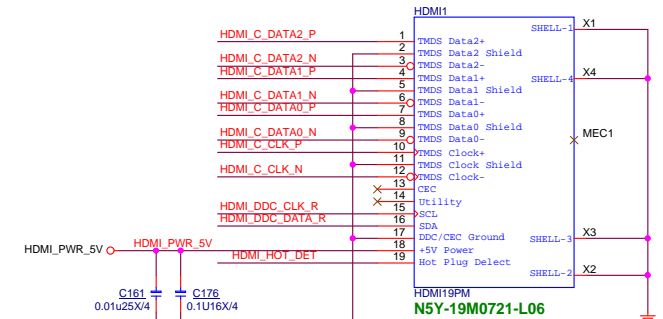
HPD



HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

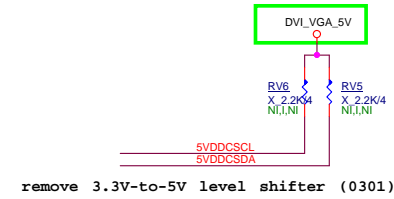
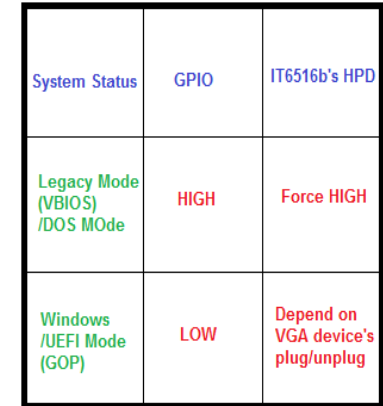


注意:耐 壓5V零件



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If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



```
remove 3.3V-to-5V level shifter (0301)
```

PCB layout diagram for the MICRO-STAR INT'L CO., LTD. MS-7B28 motherboard. The diagram shows the front panel connectors (RED, GREEN, BLUE) and their connection to the VGA and DVI ports. It includes component callouts for resistors (RV1, RV2, RV3, RV4, RV7), capacitors (CV3, CV5, CV6, CV7, CV12, CV14), and the DVI connector (X3). A table on the right lists the schematic configuration for different models (H310M Gaming, H310-A Pro). A note at the bottom right indicates a vendor suggestion for a 22ohm resistor for better I2C quality.

Schematic Cfg		Project
CFG1-7B38-H310 (H310M Gaming)	X	A
CFG1-7B38-H310-APRO (H310-A Pro)	V	B

Vendor suggest 22ohm for better I2C quality

Schematic Cfg	Project	
CFG1-7B38-H310 (H310M Gaming)	X	A
CFG1-7B38-H310-APRO (H310-A Pro)	V	B

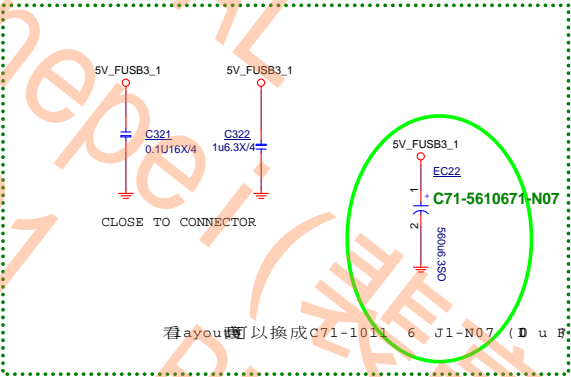
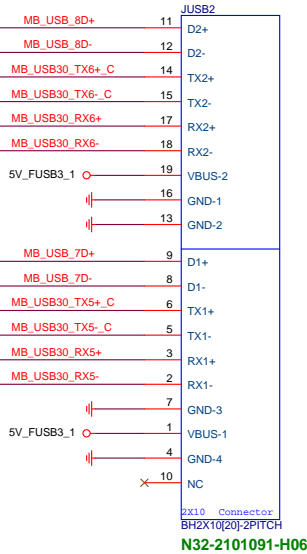
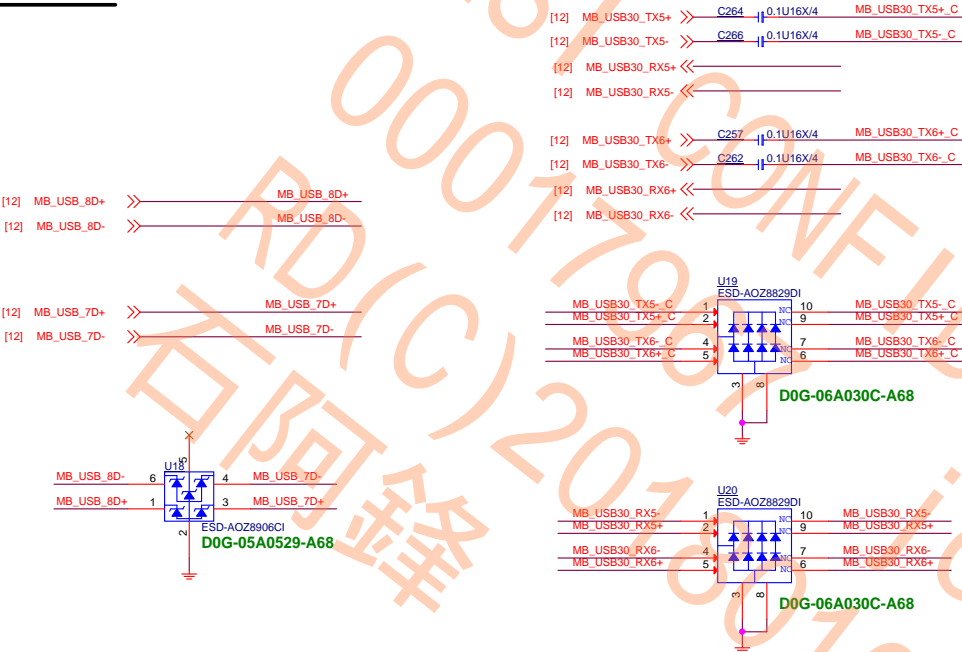


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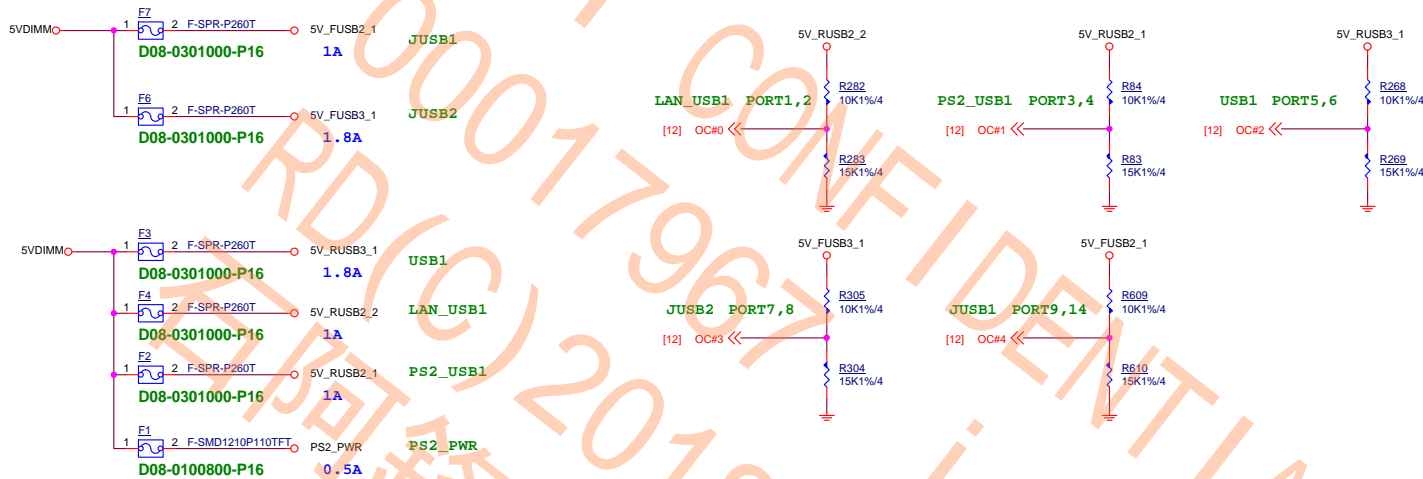
Front JUSB3 port 7,8



MICRO-STAR INT'L CO.,LTD

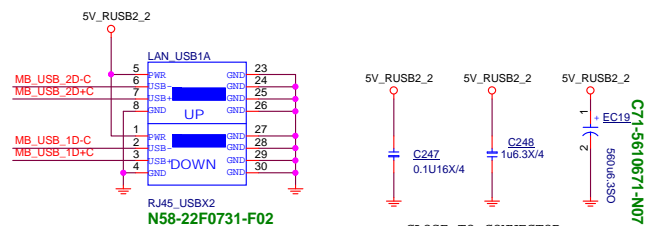
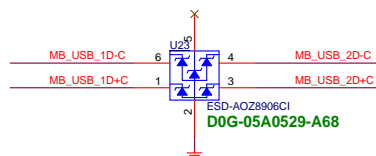
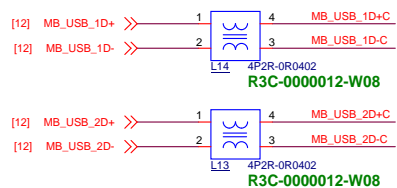
MS-7B28

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Custom		Front USB3.0 Connector	10/20/30
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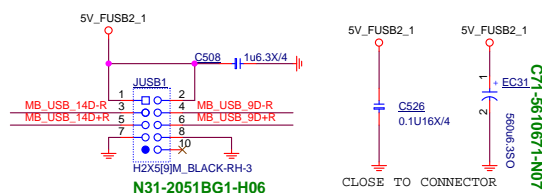
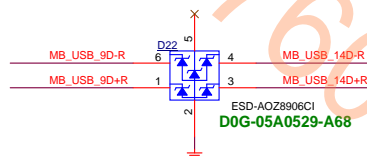
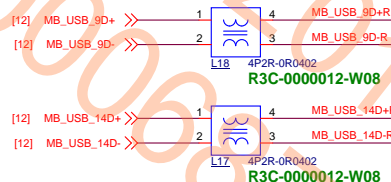


USB CONN	USB POWER	PCH PORT	OC# SIGNAL
LAN_USB1	5V_RUSB2_2	Port1,2	OC#0
PS2_USB1	5V_RUSB2_1	Port3,4	OC#1
USB1	5V_RUSB3_1	Port5,6	OC#2
JUSB2	5V_FUSB3_1	Port7,8	OC#3
JUSB1	5V_FUSB2_1	Port9,14	OC#4

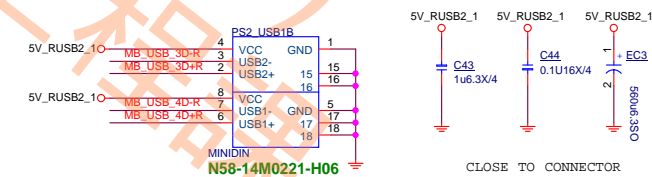
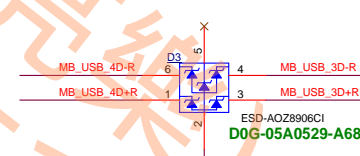
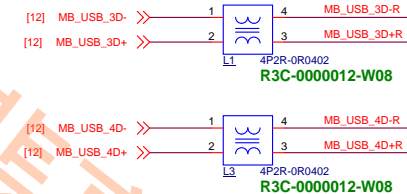
Rear USB1 port 1,2



JUSB1 PORT 9,14

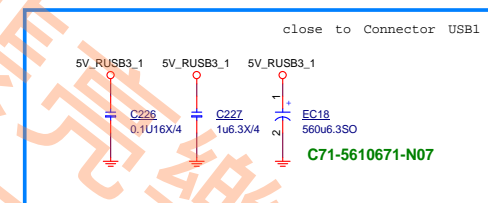
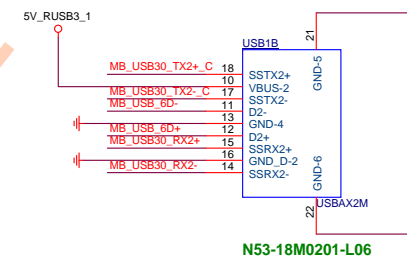
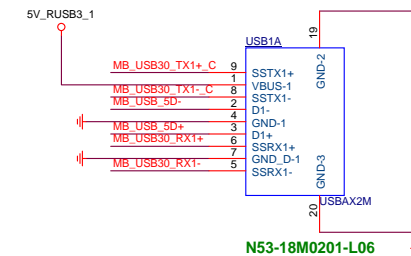
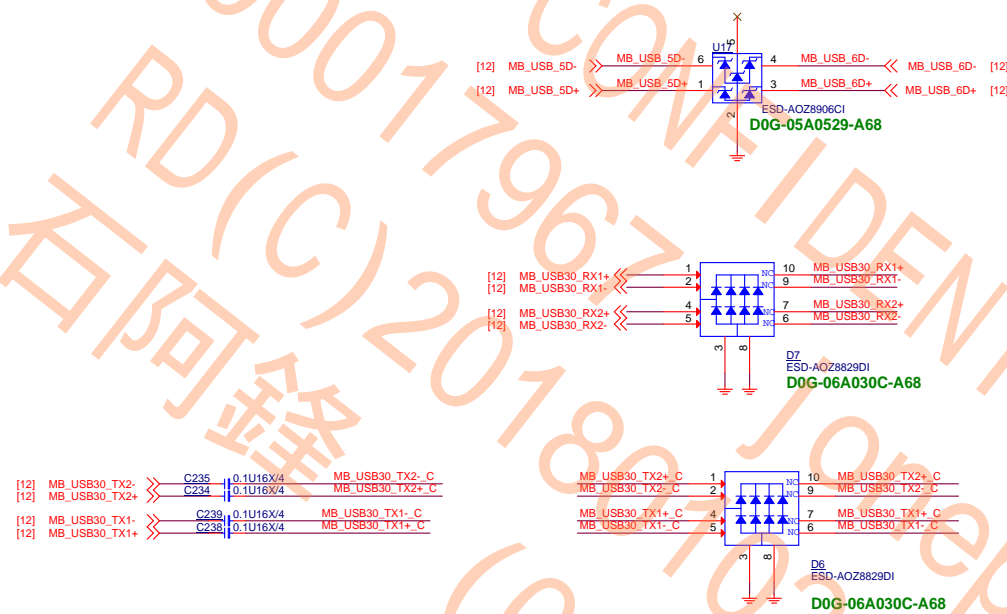


PS2_USB1 PORT 3,4



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REAR USB1 Connect

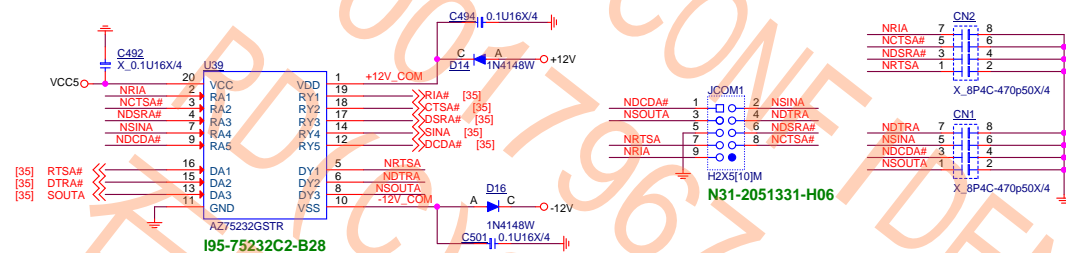


MICRO-STAR INT'L CO.,LTD

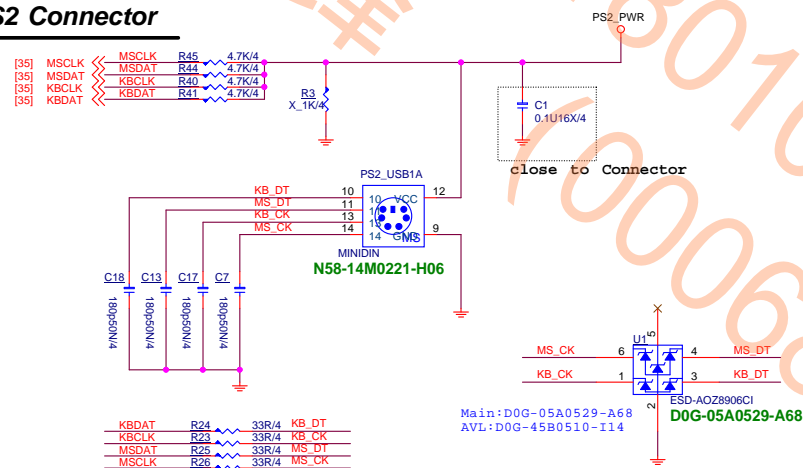
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Custom		REAR USB1 Connect	10/20/30
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SERIAL PORT 1



PS2 Connector



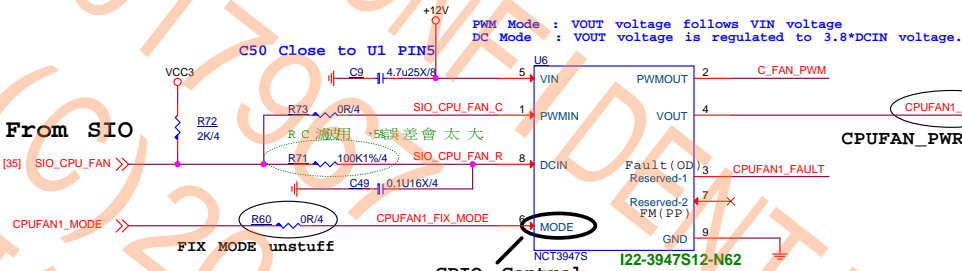
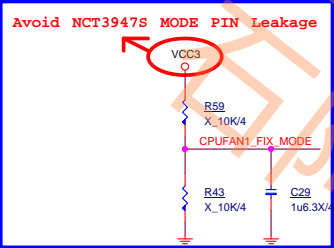
MICRO-STAR INT'L CO.,LTD

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Custom	SERIAL POR/PS2		10/29/30
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TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

GPIO 由 SIO 切换 PWM/DC 模式



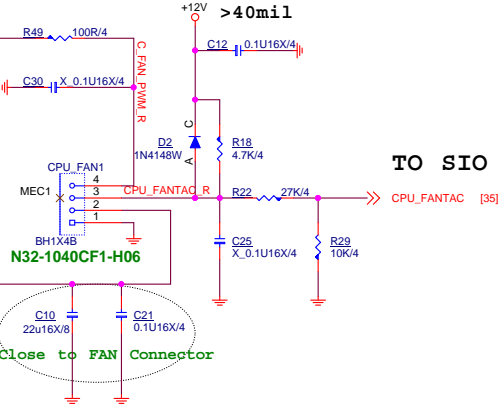
GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPIO(Floating)

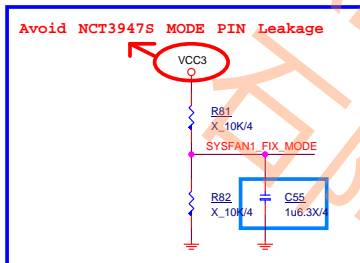
Internall pull up 1.65V

colay NCT3961

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



From SIO

[35] SIO_SYS1_FAN

[15] SYSFAN1_MODE

FIX MODE unstuff

GPIO Control

	MODE(PIN6)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internal pull up 1.65V

PWM Mode : VOUT voltage follows VIN voltage
DC Mode : VOUT voltage is regulated to 3.8*DCIN voltage.

C69 Close to U1 PINS

R C 濾用 5 時間 差 會 太 大

R62 0R/4 SIO_SYS1_FAN_C

R76 100K1%/4 SIO_SYS1_FAN_R

C50 0.1U16X/4

R74 0R/4 SYSFAN1_FIX_MODE

MODE

NCT3947S I22-3947S12-N62

colay NCT3961

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428

VCC3 R35 100K/4 SYSFAN1_FAULT

Close to FAN Connector

C11 22u16X/6 C22 0.1U16X/4

CPUFAN_PWR>40mil

N32-1040CF1-H06

BH1X4B

MEC1

SYS_FAN1

4 3 2 1

SYS1_FAN_PWM R

SYS1_FANTAC R

R19 4.7K/4

R15 27K/4

C8 0.1U16X/4

R14 10K/4

C24 0.1U16X/4

D1 1N4148W

SYS1_FAN_PWM R

R36 100R/4

C6 0.1U16X/4

SYS1_FAN_PWM R

SYS1_FAN_PWM R

SYS1_FAN_PWM R

SYS1_FAN_PWM R

SYS1_FAN_PWM R

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SYS1_FAN_PWM R

SYS1_FAN_PWM R

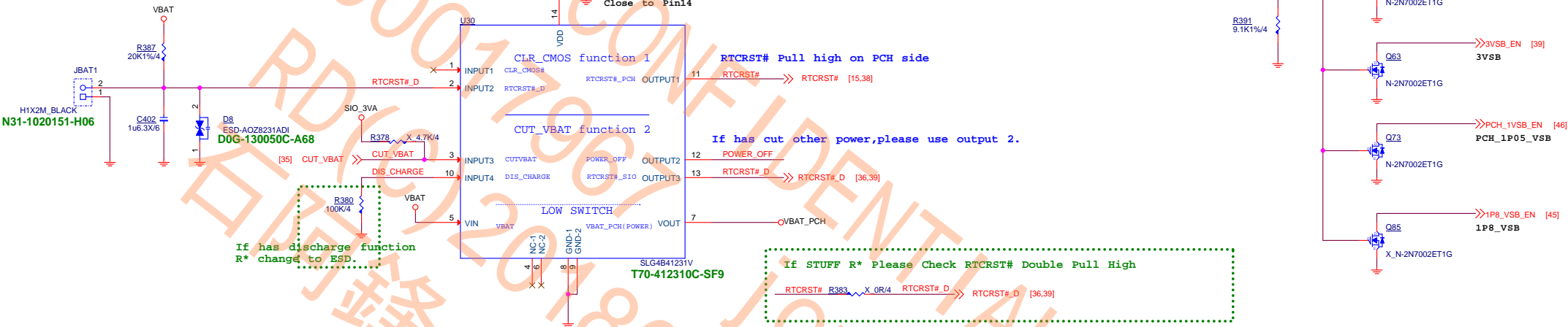
SYS1_FAN_PWM R

SYS1_FAN_PWM R

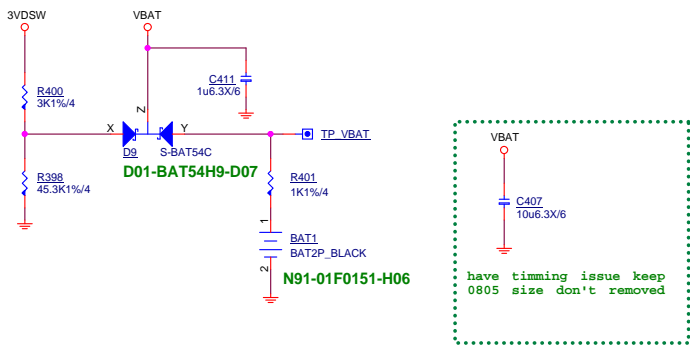
SYS1_FAN_PWM R

SYS1_FAN_PWM R

Cut VBAT



VBAT



Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

Default

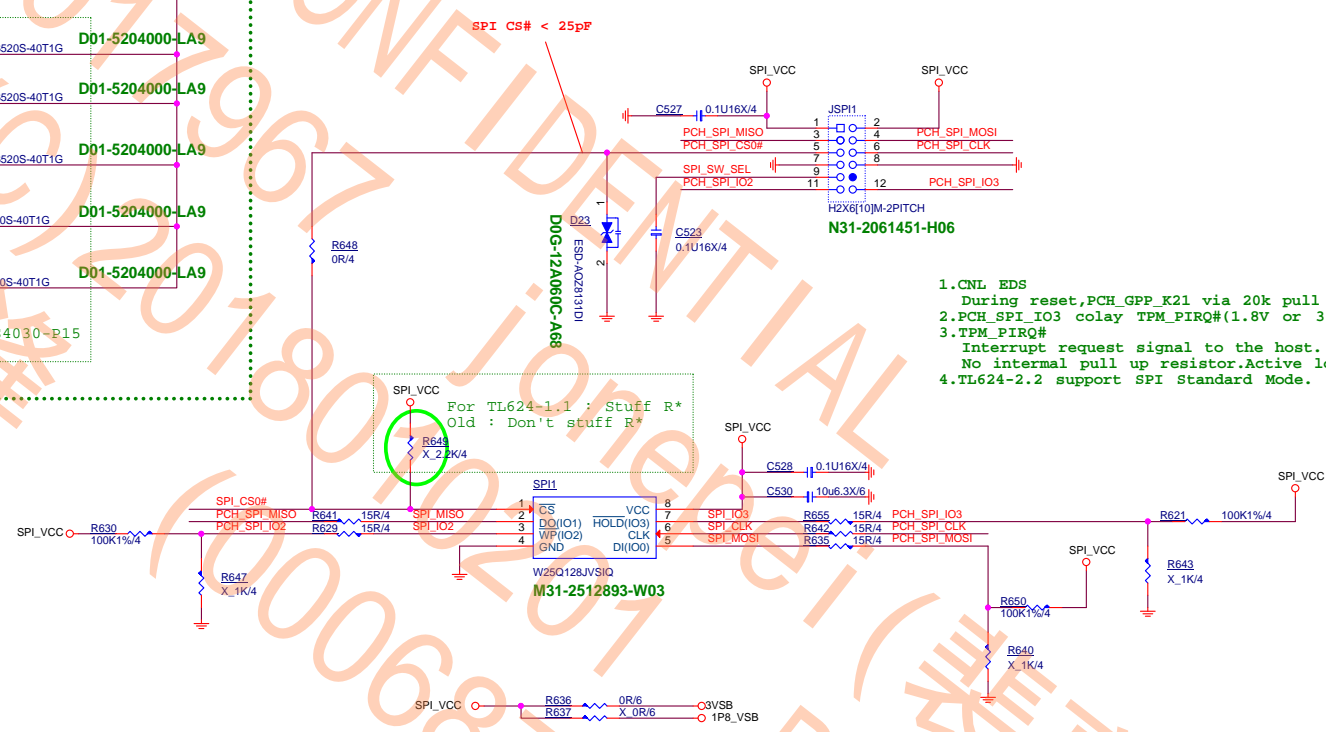
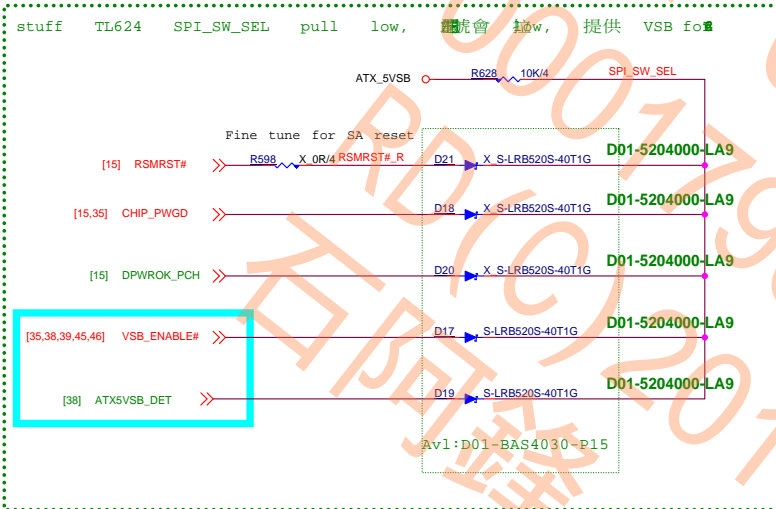


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[15] PCH_SPI_MOSI << PCH_SPI_MOSI
[15] PCH_SPI_MISO << PCH_SPI_MISO
[15] PCH_SPI_CLK << PCH_SPI_CLK
[15] PCH_SPI_CS0# << PCH_SPI_CS0#
[15] PCH_SPI_IO2 << PCH_SPI_IO2
[15] PCH_SPI_IO3 << PCH_SPI_IO3

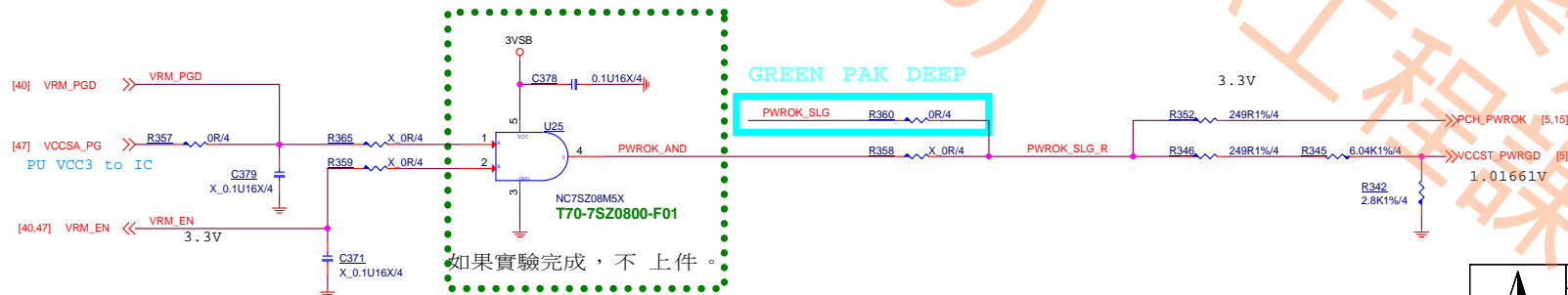
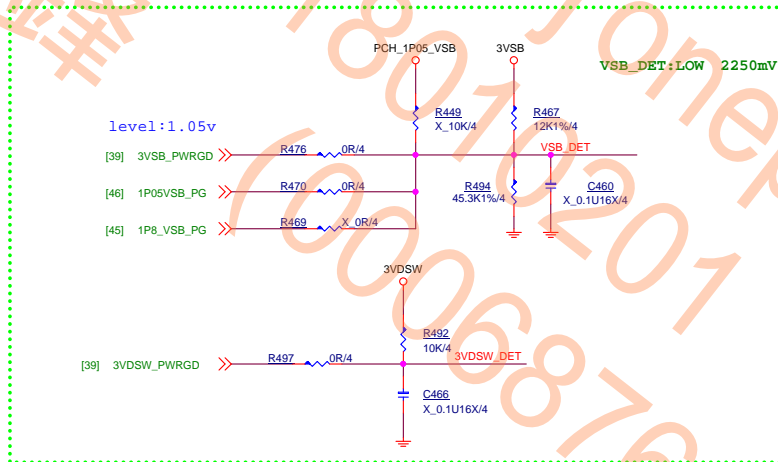
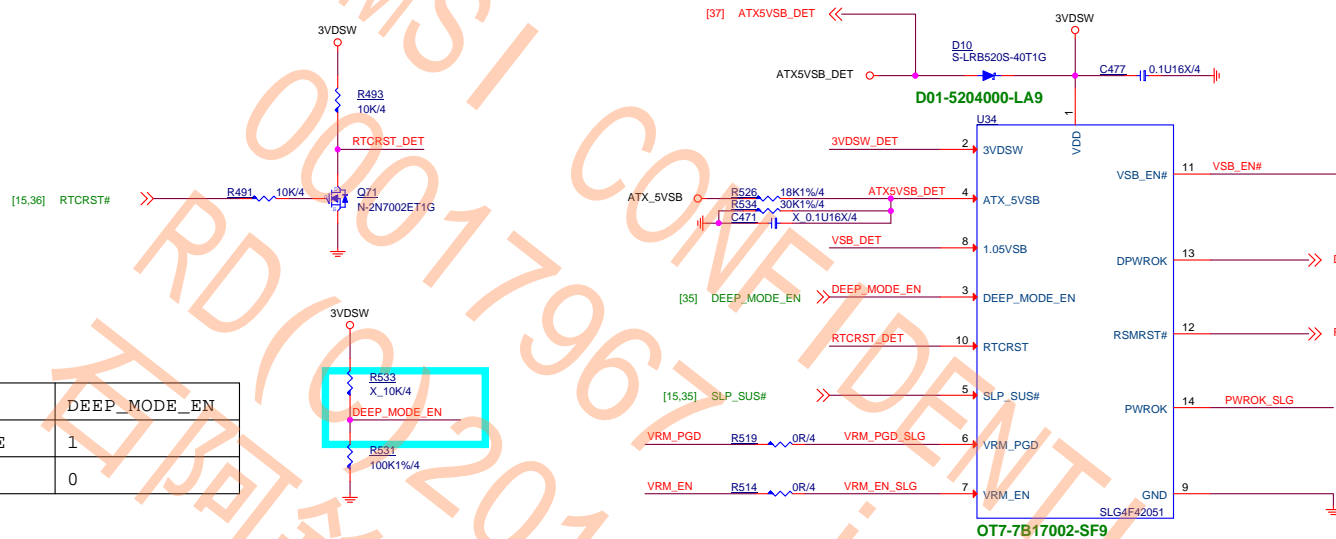


- 1.CNL EDS
During reset,PCH_GPP_K21 via 20k pull up to 3.3V.
- 2.PCH_SPI_IO3 colay TPM_PIRQ#(1.8V or 3.3V,OD)
- 3.TPM_PIRQ#
Interrupt request signal to the host.
No internal pull up resistor.Active low.
- 4.TL624-2.2 support SPI Standard Mode.



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	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0



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[illegible]

AVL: I31-0866509-A36
I31-7116S09-N03

ATX_5VSB

C416 1u6.3X/4

U31 GS7116S5

VDD VOUT

EN GND ADU

1 2 3 4 5

SIO_3V_A

C421 0.1uF6X4

3V_A_FB

R1 R403 10K1%4

R2 R407 3.16K1%4

C422 10u6.3X/6

[36] RTCRSts_D

R393 OR/4

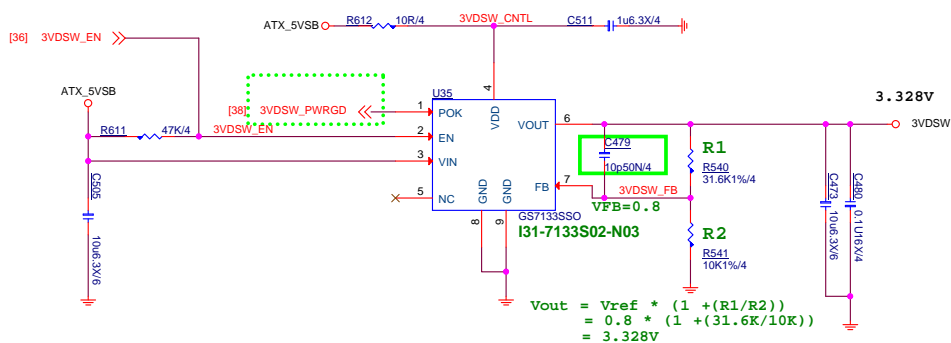
SIO_3V_A_EN

C413 X_1u6.3X/4

Vout = Vref * (1 + (R1/R2))
= 0.8 * (1 + (10K/3.16K))
= 3.33V

VFB=0.8

Intel Lan 不用小顆 C，因為瞬間電會很大。
113mA(PCH)+0.6mA(RTC)+200mA(LAN-I219)+SIO



VDDUAL is power source of 1P0SB, 1.8PSB & 3VSB

VCC5 5VSB 5V 3VSB

[35,39,49] ATX_PWR_OK

[15,35,39,40,45] SLP_S3#

[15,35,39,43,44,45] SLP_S4#

ATX_5VSB

[35,37,38,39,45,46] VSB_ENABLE#

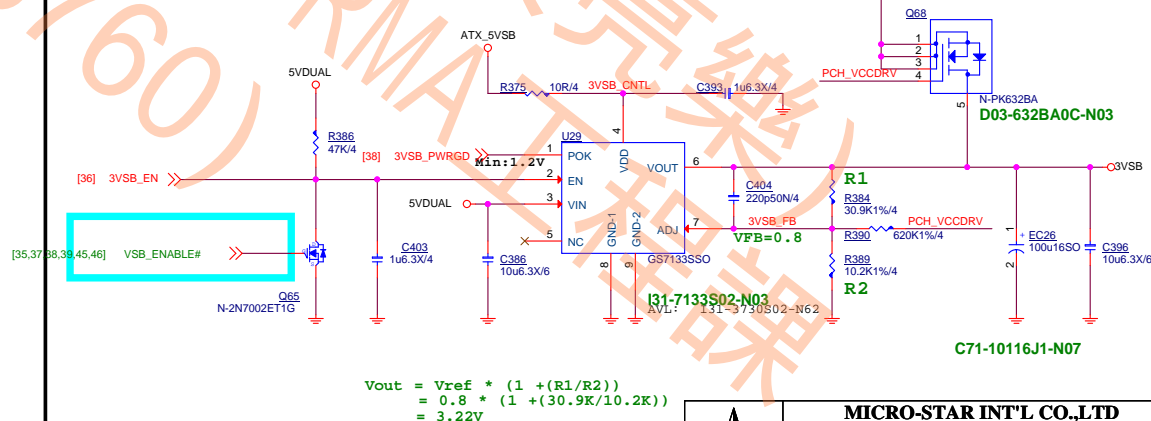
7501 Mode

H:Support S0/S3/S5

L:Support S0/S3

ATX_5VSB

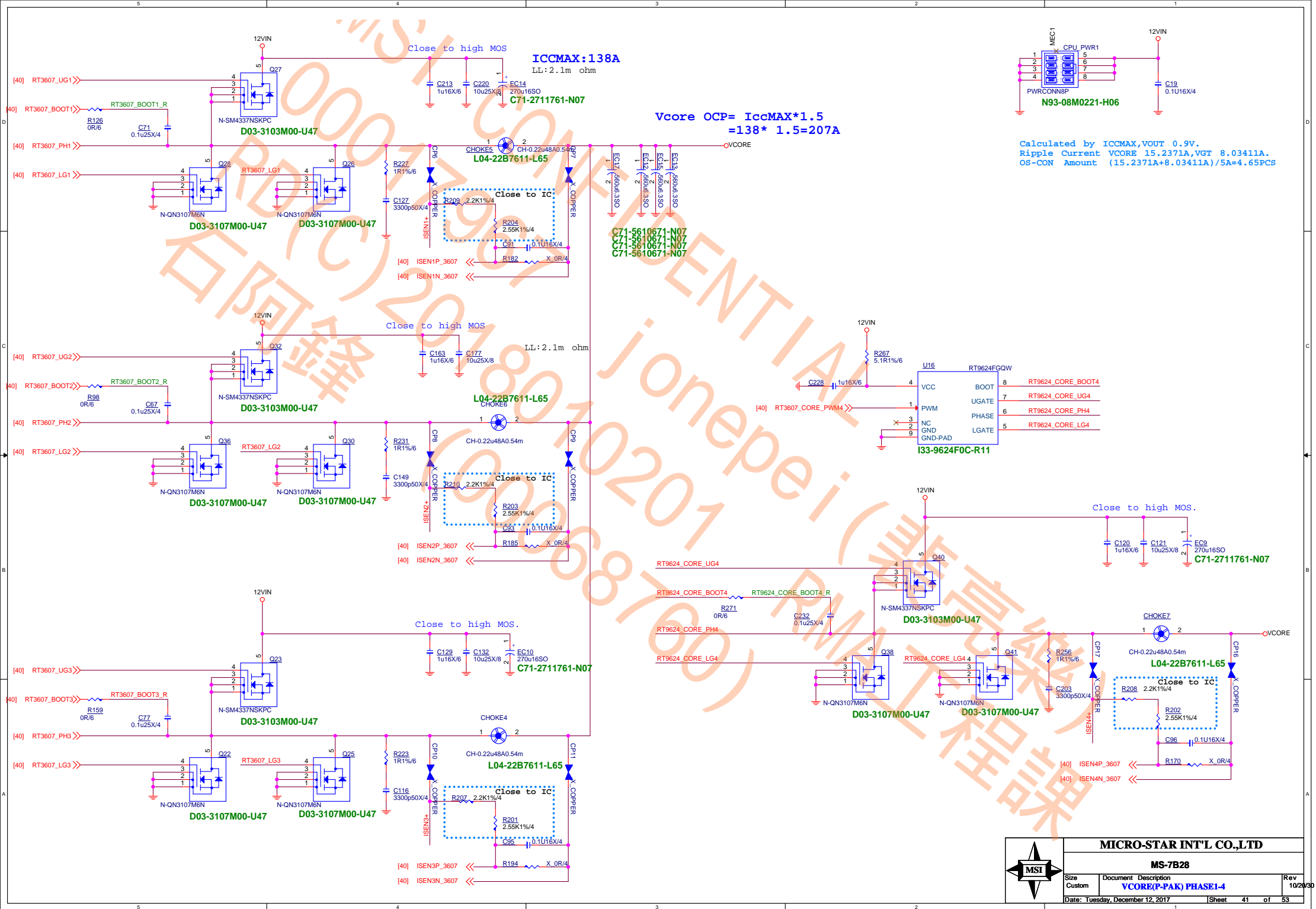
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC5 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC5 not ready and let the 3VSB sequence fail.

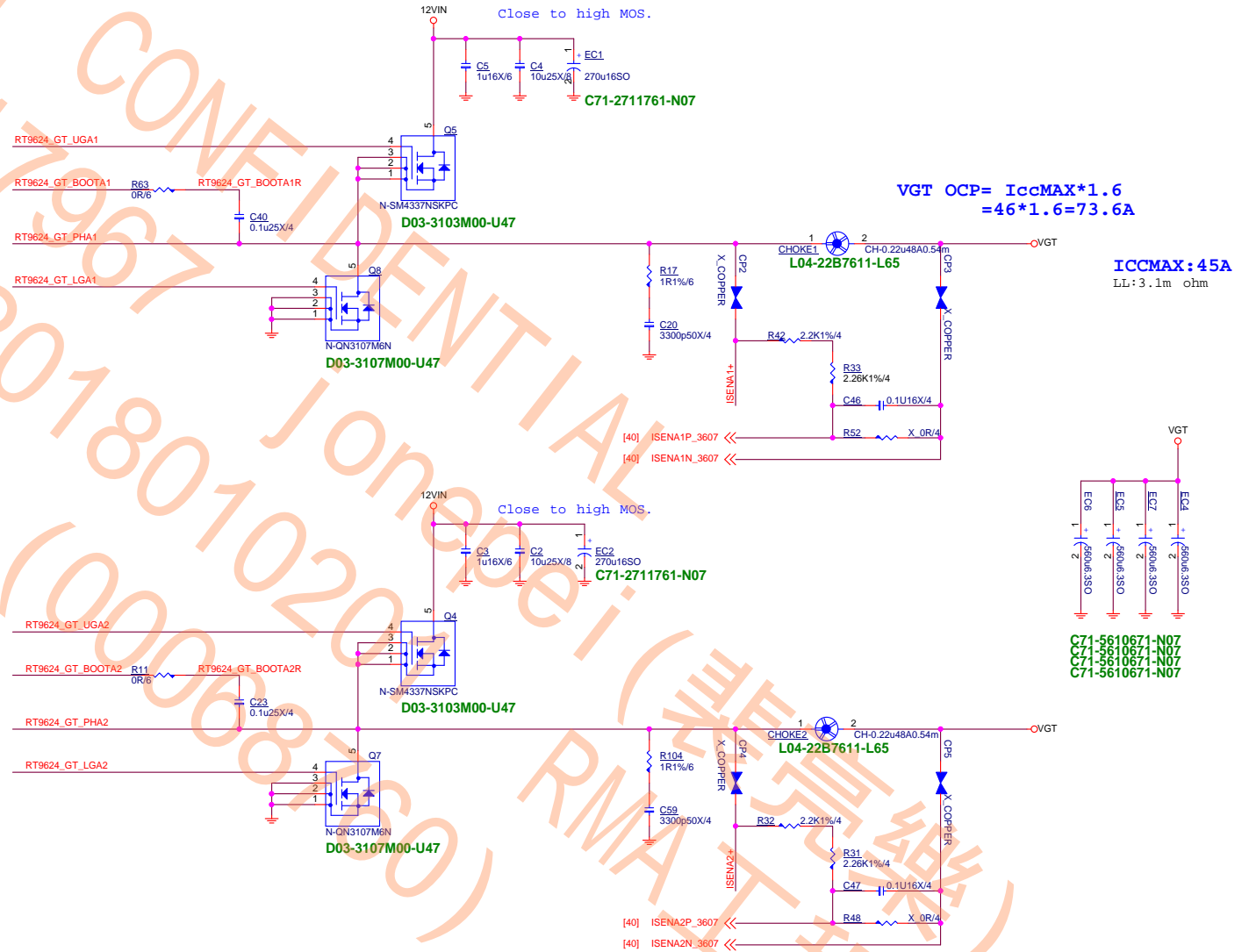
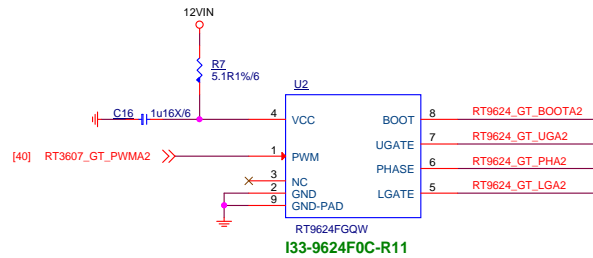
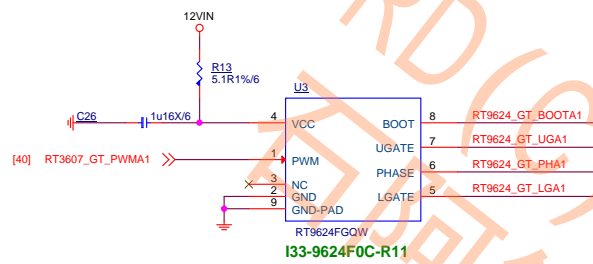
$$2.156A(PCH)+1.125A(PE \text{ SLOT} * 3)$$


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VCC_DDR@1.2V/11.525A

DDR4_1.2V 3.3A+ 7.85A+0.375A=11.525A

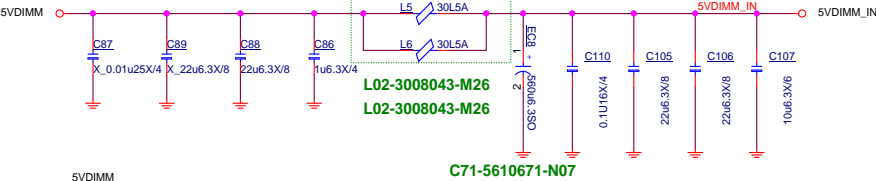
3.3A FOR CPU
10A FOR 2DIMM DDR4
0.375A FOR VTT_DDR

Rlimit = Llimit * Rds * 10 /5uA
Rlimit = 14.9825*4*10/5

D03-632BA0C-N03
Current limit= 118K*5uA/10/4mohm=14.75A
0.4V<=Rlimit *5uA<=3V

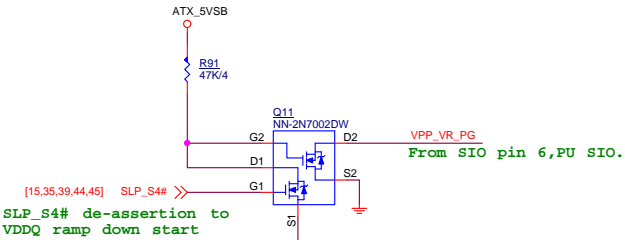
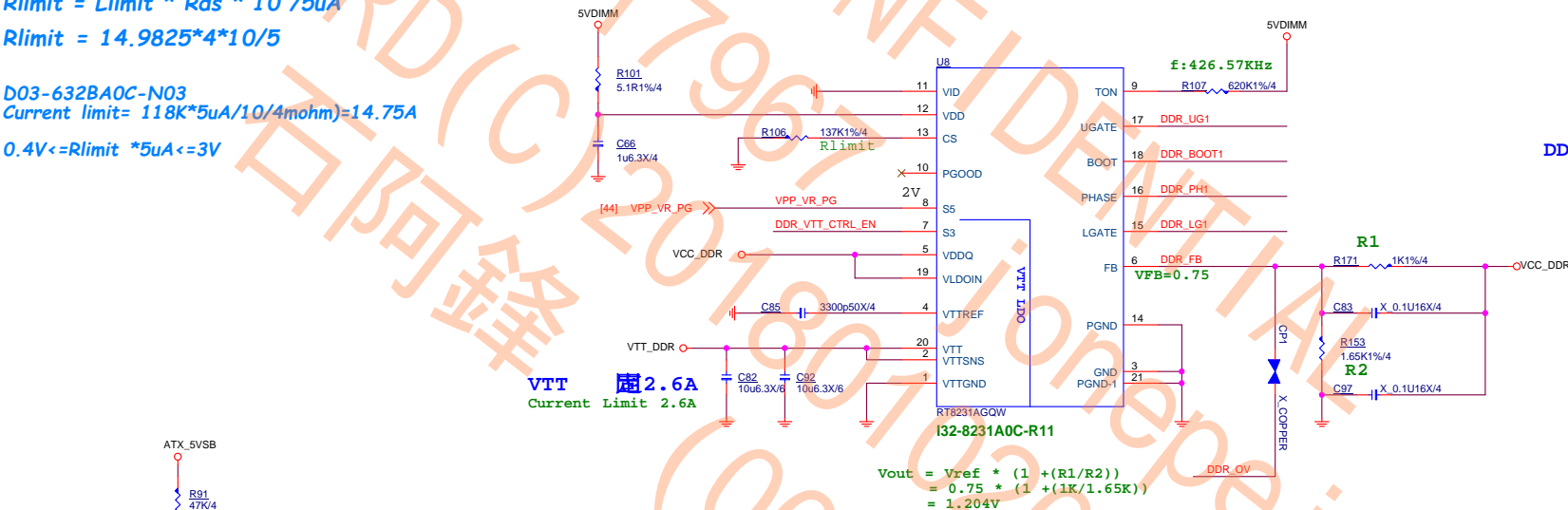
VID	Reference Voltage (V)
H	0.675
L	0.75

Input Current= (11.525A*1.2V)/5V/0.8=3.4575A
L02-3008043-M26
Over 85°C Rated Current 1.5A.

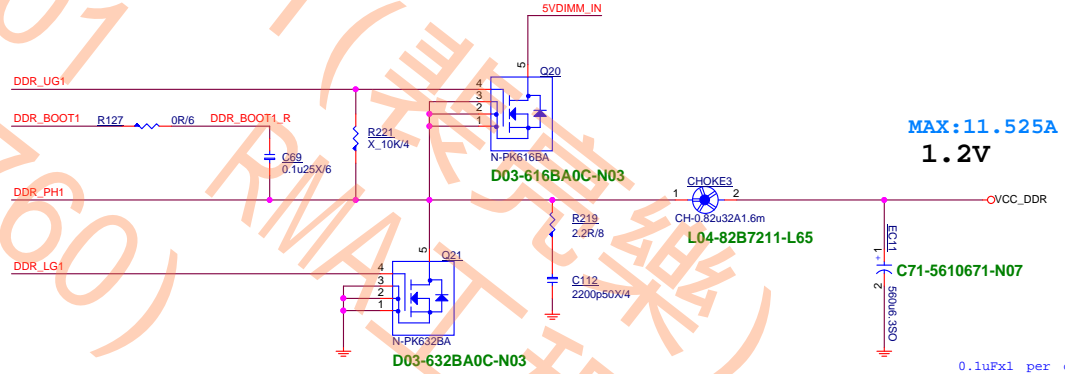
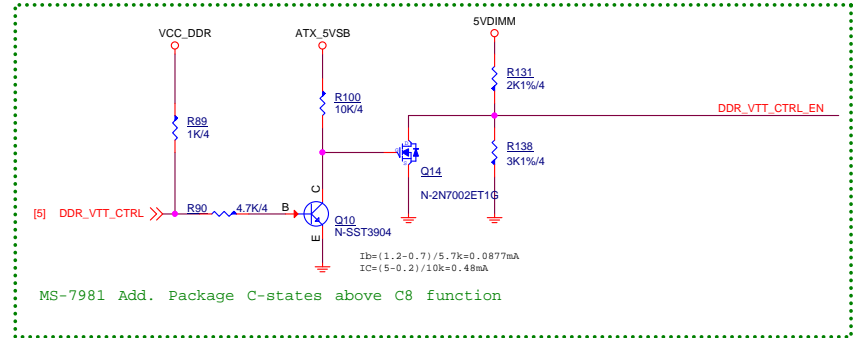


Irms = Iout * SQRT((Vout/Vin) * (1-(Vout/Vin)))
=11.525* 0.427
= 4.921175A

DDR OCP= R44*5uA/10/Dds(on)
138k*5uA/10/3m=23A
138k*5uA/10/4.6m=15A
MOS Rds(on)是m~4.6m ohm

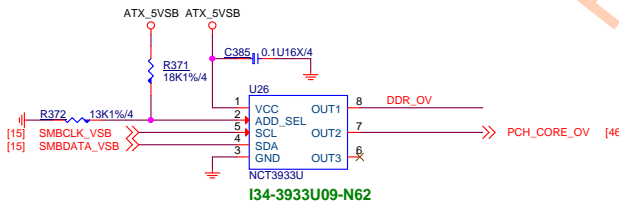


VPP ramp down after VDDQ ramp down



UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



VPP25 @2.5V/2A

2DIMM :1.12A FOR
DDR VPP2.5V

DDR VPP 4.8

Switch Frequency
Default 1.2MHz
Current Limit 4.8A.

Input Current= (2A*2.5V)/5V/0.8=1.25A

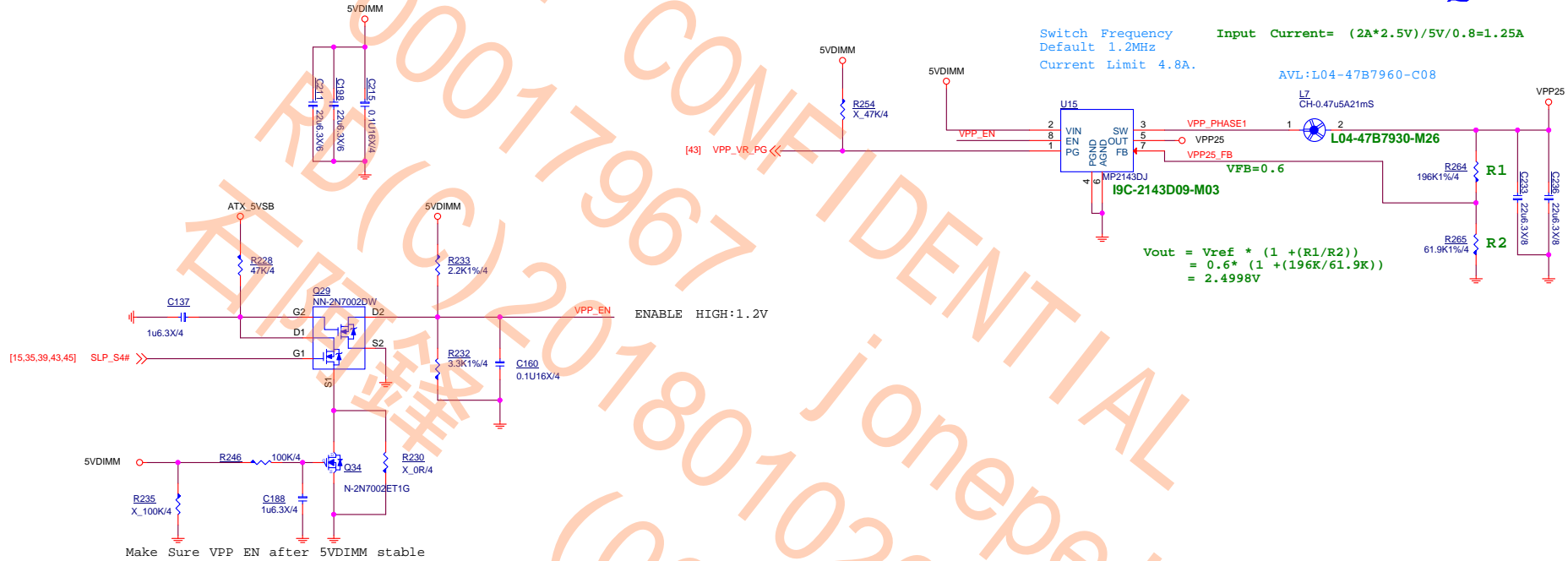
AVL:L04-47B7960-C08

LZ
CH-0.47uA21mS

L04-47B7930-M26

VFB=0.6

$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.6 * (1 + (196K/61.9K)) \\ &= 2.4998V \end{aligned}$$

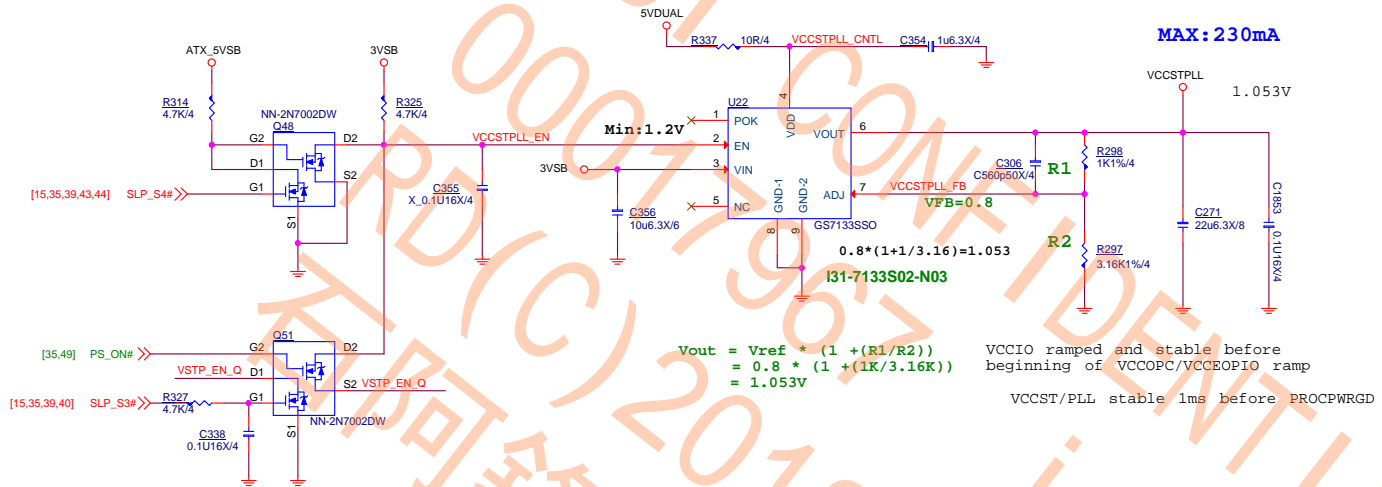


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Custom	DDR-MP2143-VPP25		10/20/30
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VCCSTPLL@1.05V/230mA

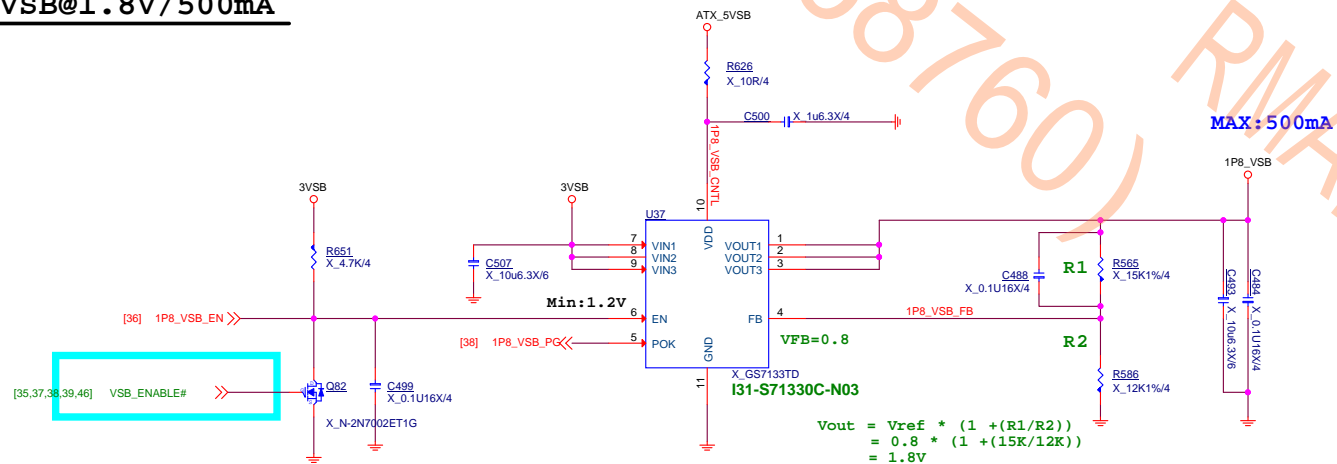


$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (1K/3.16K)) \\ &= 1.053V \end{aligned}$$

VCCIO ramped and stable before beginning of VCCOPC/VCCOPPIO ramp

VCCST/PLL stable 1ms before PROCPPWRGD

1P8_VSB@1.8V/500mA



$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (15K/12K)) \\ &= 1.8V \end{aligned}$$



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Size	Document	Description	Rev
Custom	CPU PWR ST/PLL		10/20/30
Date:	Tuesday, December 12, 2017	Sheet	45 of 53

PCH_1VSB@1.05V/11.981A

D03-632BA0C-N03

Current limit= $5.6k \times 10uA / 4mohm = 14.75A$

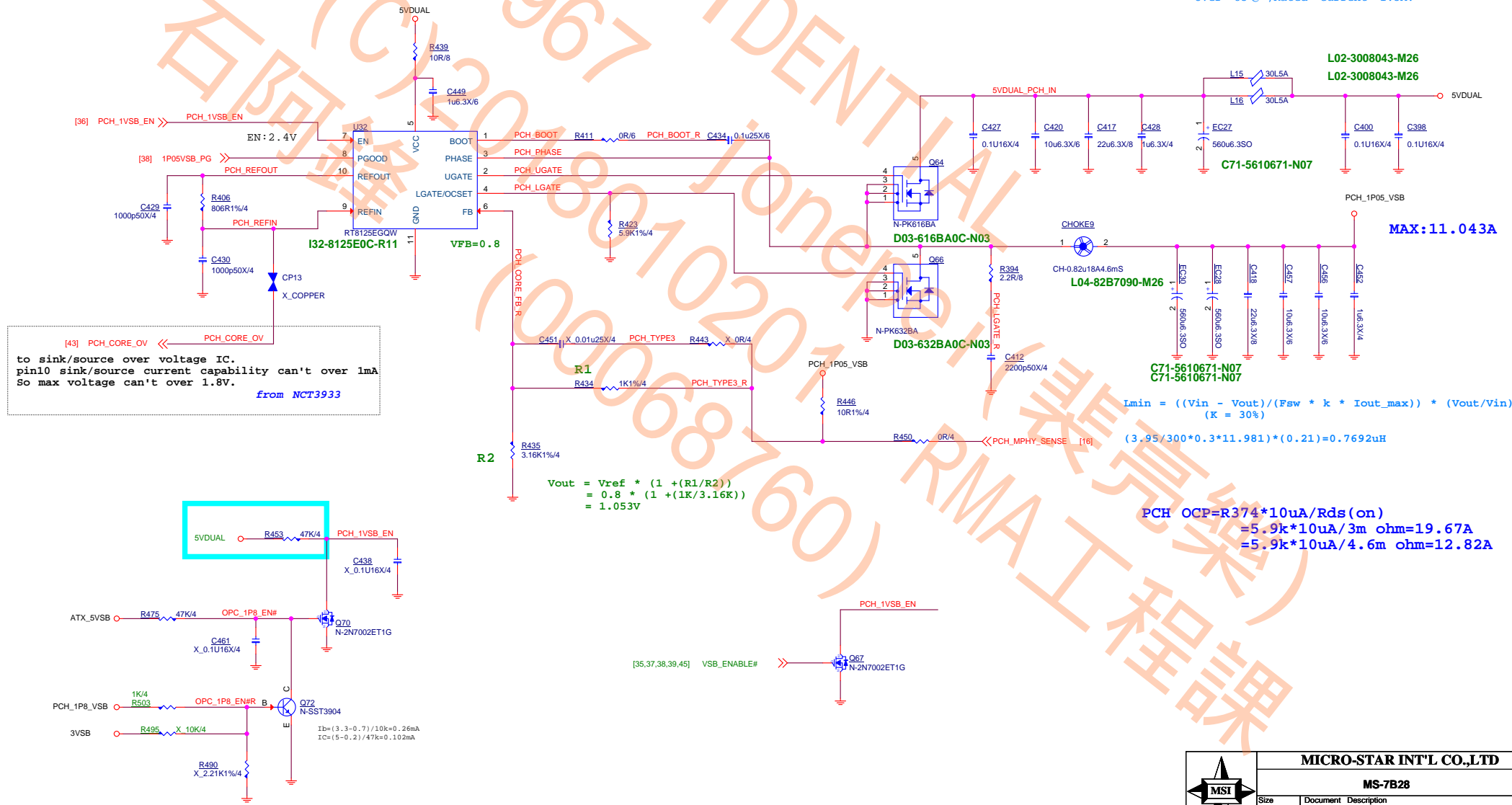
$$I_{rms} = I_{out} \times \sqrt{((V_{out}/V_{in}) \times (1 - (V_{out}/V_{in})))}$$

$$= 11.981 \times 0.407$$

$$= 4.876A$$

$$I_{in} = 11.043A \times 1.05V / 0.8 / 5V = 2.898A$$

Over 85°C ,Rated Current 1.5A.



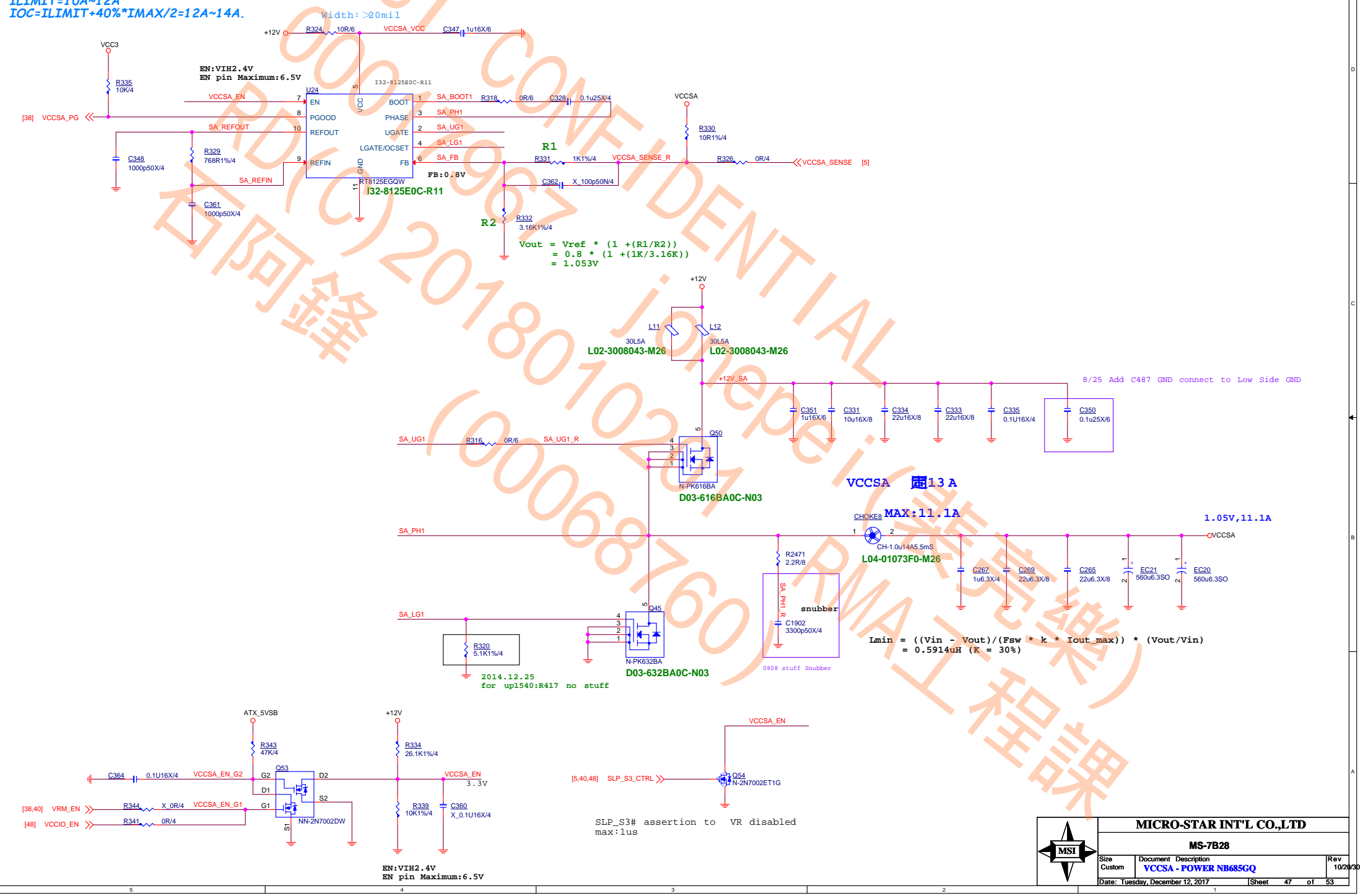
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Size	Document	Description	Rev
Custom		PCH Core power	10/20/30
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VCCSA@1.05V/11.1A

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

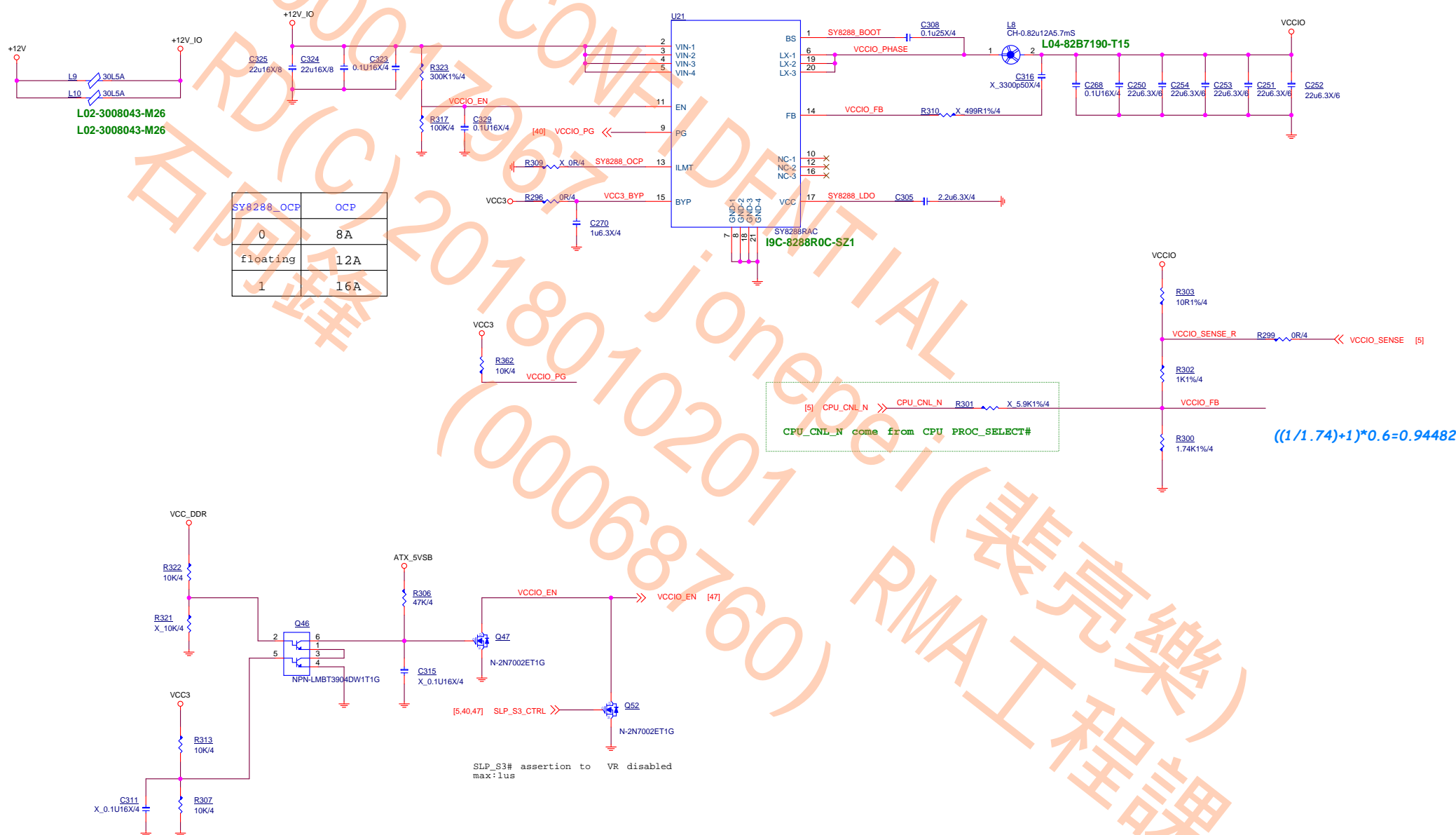


VCCIO@0.95V/6.4A

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

VCCIO 定12A(floating

MAX: 6.4A



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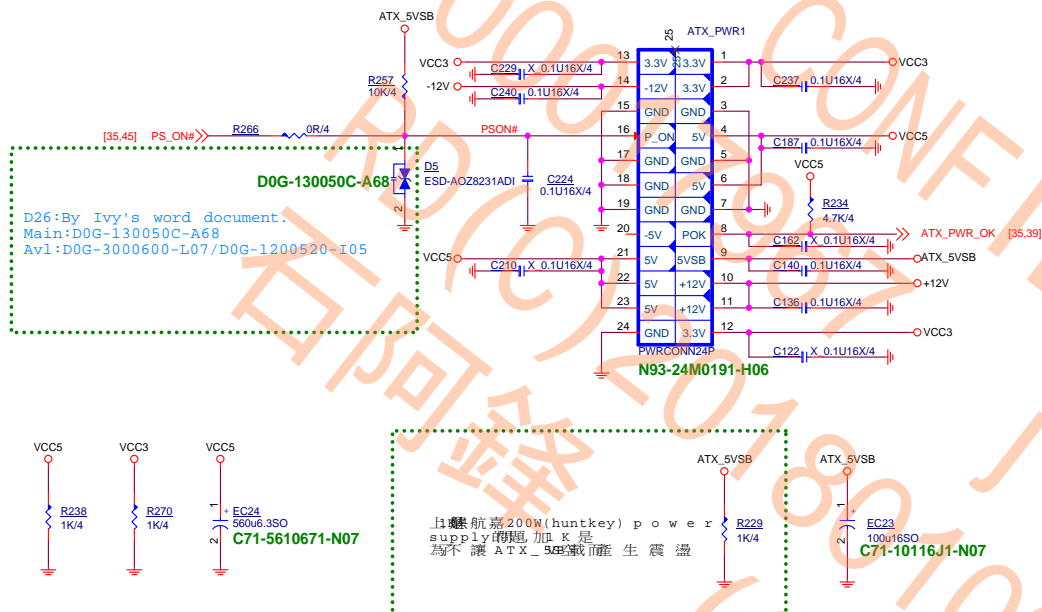
MS-7B28

Size	Document Description
Custom	VCCIO - POWER SY8288

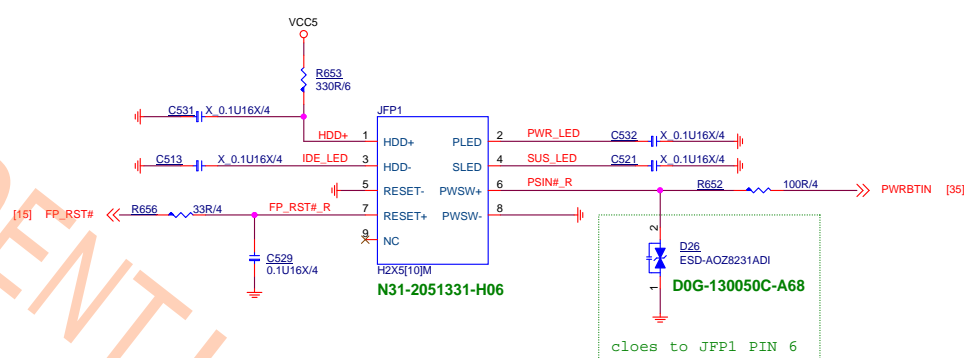
Size Custom	Document Description VCCIO - POWER SY8288	Rev 10/20/30
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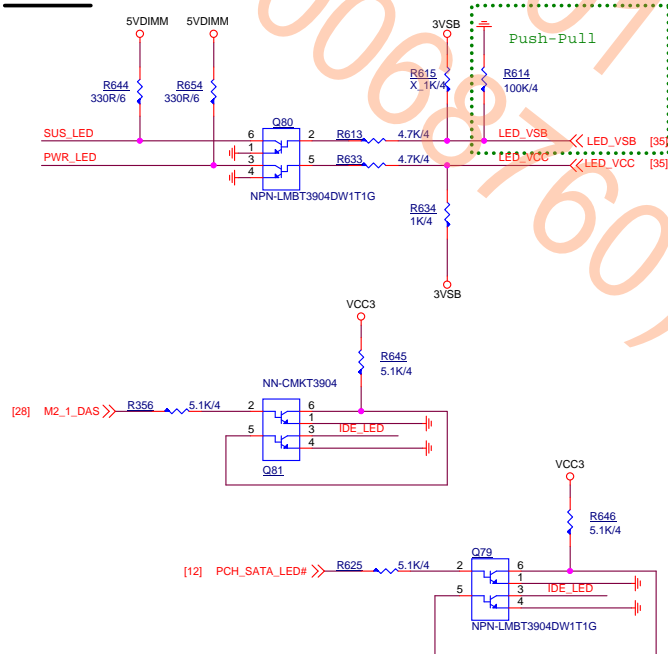
ATX POWER CONNECTOR



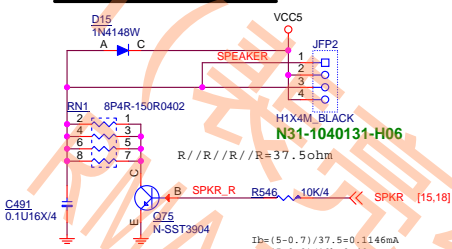
FRONT PANNEL



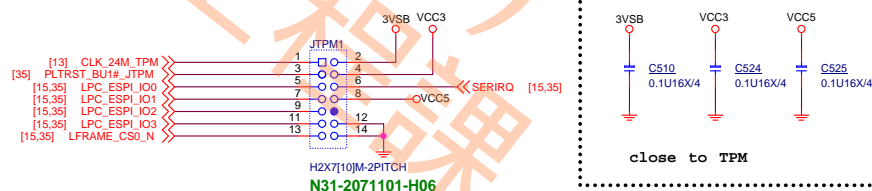
LED



Speaker Pin Header



TPM



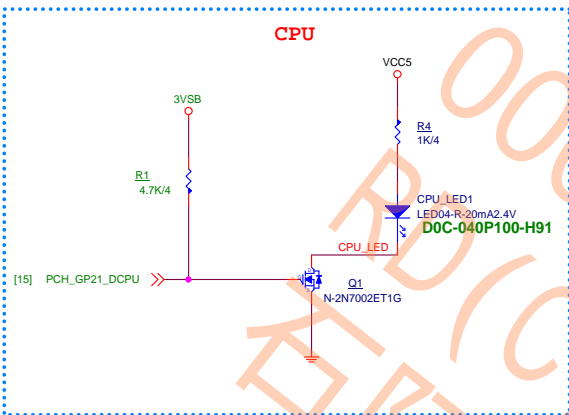
MICRO-STAR INT'L CO.,LTD

MS-7B28

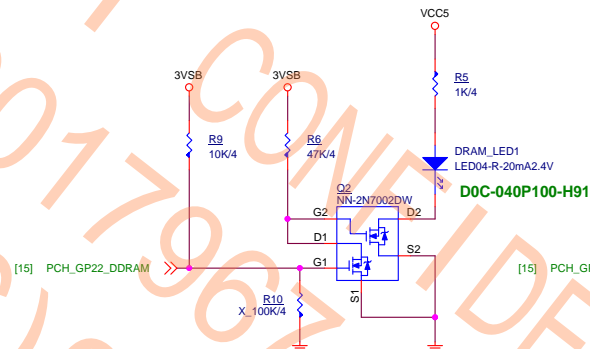
Size Custom	Document Description ATX F_Panel/TPM/MSI_LED	Rev 10/20/30
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EZ DEBUG LED

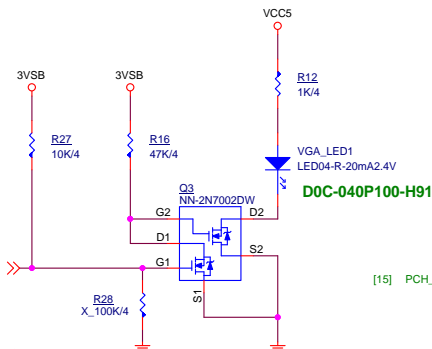
CPU



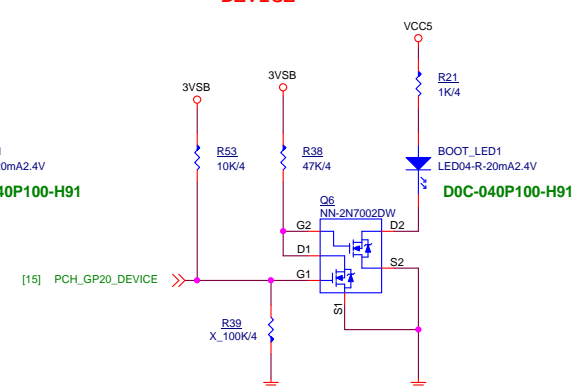
DRAM



VGA



DEVICE



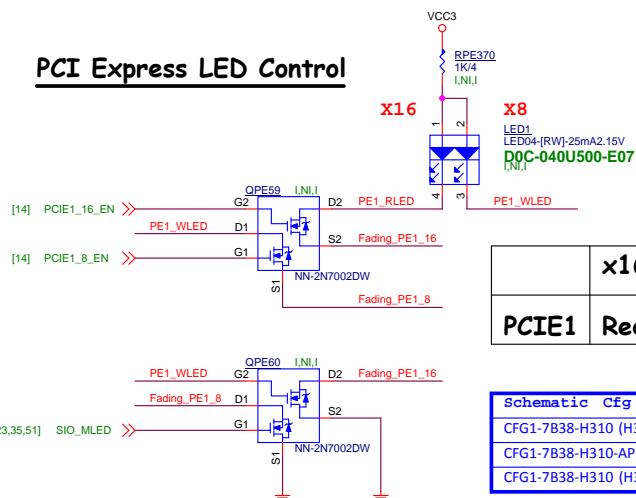
LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

LED

RED:D0C-040P100-H91
AVL:D0C-040S500-E07

WHI:D0C-040T200-H91
AVL:D0C-040S200-E07

PCI Express LED Control



	x16	x8
PCIE1	Red	White

Schematic Cfg	Project
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	V A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	X B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	V C

- 開機斷電狀態下，3個LED先維持 default 暗開機電後
1. 首先進行 CPU check CPU LED 亮，check PASS 後則 CPU LED 滅掉
 2. 接著依序進行 Memory / memory LED 亮 check PASS 後則 memory LED 滅掉
 3. VGA 的 check / VGA LED 亮，check PASS 後則 VGA LED 滅掉
 4. 因此最後正常順利開機後，三個 LED 都滅掉的。
- (系統重啟或其他原因造成系統重開機則重複上述流程)



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Size	Document	Description	Rev
Custom	ALL LED Control		10/20/30
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OPTION BOM PARTS

Schematic Cfg	Project
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	C

5010 Level

A
EZ Debug LED
OPT EZ GPLUS
LED04-R-20mA2-4V_1608-HF
D0C-040P100-H91
Red
PD0-07B2810-E48
PD0-07B2810-G37
OPT PCB GPLUS
7B28_10

B
EZ Debug LED
OPT EZ PRO
LED04-R-20mA2-4V_1608-HF
D0C-040T200-H91
White
PD0-07B2820-E48
PK0-07B2820-G37
OPT PCB PRO
7B28_20

C
EZ Debug LED
OPT EZ GARCTIC
LED04-R-20mA2-4V_1608-HF
D0C-040T200-H91
White
PD0-07B2830-E48
PS0-07B2830-G37
OPT PCB GARCTIC
7B28_30

PCB

5020 Level

A
AUDIO LED
OPT AUDLED GPLUS
LED04-W-20mA3.25V
USB_C1_24_2
D0C-040S600-E07
Red

B
X

C
AUDIO LED
OPT AUDLED GARCTIC
LED04-W-20mA3.9V_1608-RH
USB_C1_24_2
D0C-040T300-H91
White

60 Level

A
REAR U3
OPT REARU3 GPLUS
LANE_U3
USBAX2M_RED-RH-2
USB_C1_24_2
N53-18M0201-L06

B
REAR U3
OPT REARU3 PRO
LANE_U3
USBAX2M_BLUE-RH-6
USB_C1_24_2
N53-18M0091-F02

C
REAR U3
OPT REARU3 GARCTIC
LANE_U3
USBAX2M_RED-RH-2
USB_C1_24_2
N53-18M0201-L06

DDR Slot
OPT DDRLSLOT GPLUS
DDRIV_288P
DDRIV_D288
N13-2880681-L06

DDR Slot
OPT DDRLSLOT PRO
DDRIV_288P
DDRIV_D288
N13-2880561-L06

DDR Slot
OPT DDRLSLOT GARCTIC
DDRIV_288P
DDRIV_D288
N13-2880521-L06

PCIEx16 Slot
OPT PCIE16 GPLUS
PCIEX_16
SLOT-PCI164P_RED-2PITCH-RH-1
N11-1641671-L06

PCIEx16 Slot
OPT PCIE16 PRO
PCIEX_16
SLOT-PCI164P_BLACK-2PITCH-RH-38
N11-1641221-L06

PCIEx16 Slot
OPT PCIE16 GARCTIC
PCIEX_16
SLOT-PCI164P_WHITE-2PITCH-RH-4
N11-1641601-L06

DVI
OPT VGA GPLUS
VGA
DVI24P_BLACK-RH-17
N5B-24F0771-EB6

DVI
OPT VGA GARCTIC
VGA
DVI24P_BLACK-RH-17
N5B-24F0771-EB6

VGA+DVI
OPT VGADVI PRO
VGA+DVI
VGA_DVI-RH-31
N58-39F0371-EB6

PACK LABEL
OPT LA GPLUS
B310
Label
MKT
G51-M1SPM62-Q13

PACK LABEL
OPT LA PRO
B310
Label
MKT
G51-M1SPM61-Q13

PACK LABEL
OPT LA GARCTIC
B310
Label
MKT
G51-M1SPM60-Q13



MICRO-STAR INT'L CO.,LTD		
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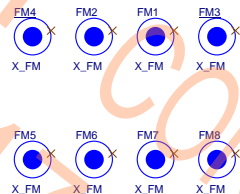
HS_PCH1

PCH
heatsink

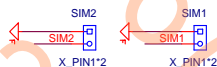
E31-0408580-K08
HS-0408580

申請 中

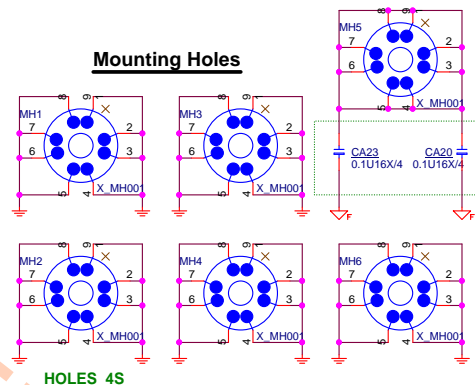
Optical Fiducial Marks-120



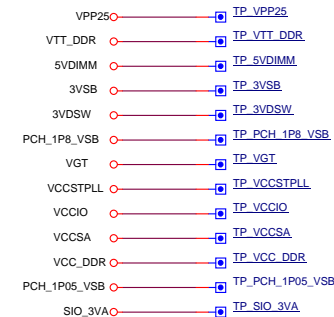
Simulation



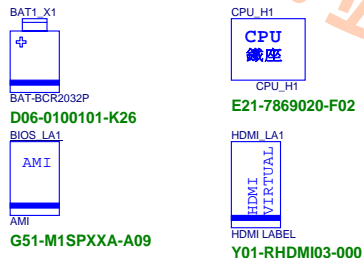
Mounting Holes



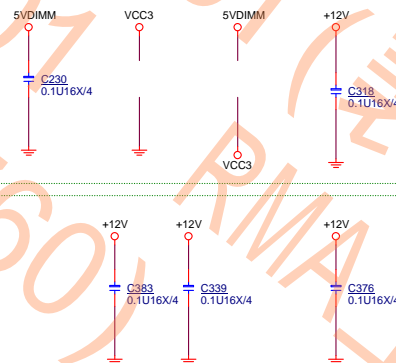
HOLES_4S



Near SIO CHIP



return path



For M2 reference +12V USE
please close to under M2